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Characteristic of I-V , C-V for a-Ge:Sb/c-GaAs Hetrojunction

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Abstract: Ge:Sb films with thickness (500nm) have been deposited by thermal evaporation technique on glass substrate and c-GaAs wafer at room temperature, under vacuum of 10^{-5} mbar with rate of deposition equal to 10Å/sec. These films have been annealed at different annealing temperatures (100, 200)^{0}C. The structural characteristic of the films prepared on glass and GaAs substrates have been studied by using X-ray diffraction, the tests show that all the films have amorphous structure for all annealing temperatures. The C-V measurement of a-Ge:Sb/c-GaAs heterojunciton at frequency 1 KHz and we found built – in potential (V_{bi})increase from 0.645 V to 0.84 V with $T_a$increase from RT to 200 ^{0}C. Also from I-V characteristic we found that the quality factor decreases from 2.641 to 2.358 for same annealing temperature, this may be interpreted in term improvement of crystal structure with heat treatment.

Keywords: Control, routing, communication network.

1. Introduction

Hetrojunction devices of amorphous-crystalline types have been much attention from researcher's studies, because of their potential as wide or narrow band gap in application of thin film transistor, hetrojunction and solar cells a-Si/c-Si, a-Ge/c-Si [1-2].These hetrojunction have widely been studies in Si technology during the last decade since varying properties can be achieved by charging prepared condition as substrate temperature, thickness and annealing temperature [3].Many authors group studies the current-voltage of the junction between c-GaAs/c-Si in field solar cells can proved power for satellites [4]. amorphous thin films possess a large density of dangling bonds, which defect doping attempts because dopant attach themselves to these bonds, but by improvement the prepared condition can illumination these defect and hydrogenation of films to reduce the dangling bond [5]. The purpose of this study is to fabricate the a-Ge:Sb/c-GaAs junction and investigate I-V and C-V characteristic as a function to annealing temperature and built in potential V_{bi}.

2. Experimental Procedure

a-Ge:Sb thin film were prepared by thermal evaporation technique in vacuum system supplied by Balzers model(BL510). In order to preparation the hetrojunction, thin film a-Ge:Sb deposited on c-GaAs.

All samples were prepared under constant condition (presser, substrate temperature and rat of deposition); the main parameter that control the nature of the film properties is thickness (0.5µm) and annealing temperature (RT,100,200)^{0}C.

The structure of the Ge:Sb film grown on GaAs substrate has been examined by X-ray diffraction using a Philips X-ray diffractometer system. The source of radiation was Cu(Kα) with wave length λ=1.5406Å , the current was 30mA and the voltage was 40KV.

The capacitance of the hetrojunction was measured as a function of the reverse bias voltage at the range (0 to -14) Volt with fixed frequency of 1kHz by using HP-R2C unit model 4274A multi-frequency LCR meter.

Current voltage measurements were made for a-Ge:Sb/c-GaAs hetrojunction when they were exposed to halogen lamp light Philips 120W with different intensities (69.2 ,105 , 183) mW/cm^2 using keithly digital electrometer 616 , voltmeter and D.C power supply under forward and reverse bias voltage which was in the range (-1.8 – 2.2) Volt .

3. Results and Discussion

The XRD results of Ge films prepared on glass at substrate temperature equal to room temperature for different annealing temperatures (RT, 100, 200)^{0}C, are shown in Fig. (1)

We observed that Ge:Sb films are amorphous structure where no peaks appear, similar variation repeated by H.Howari [6].

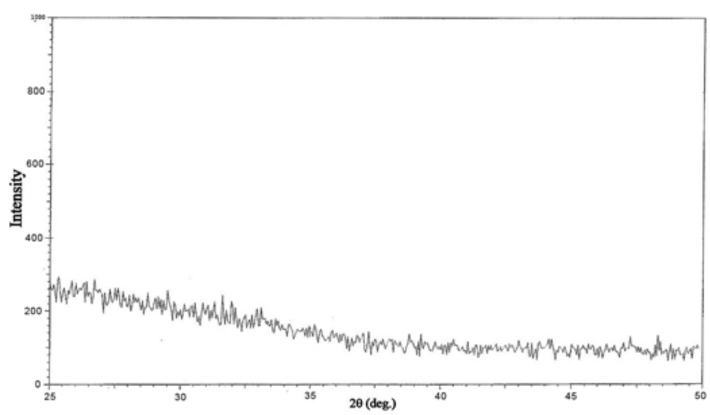


Figure 1: X-ray diffraction of a-Ge:Sb films for different annealing temperatures.

Fig (2) shows C-V characteristic for aGe:Sb/c-GaAs hetrojunction at reverse bias voltage (0 to -1.4) Volt and constant frequency 1kHz for different annealing temperature (RT, 100, 200)^{0}C, We can notice from this figure that the value of capacitance decreases with increases of the revers bias voltage and annealing temperature. This behavior attributed to the increasing in the depletion region width which leads to increase the value of built in potential.

The value of built in potential can be found from the plots the relation between $1/C^2$ and the revers bias voltage , and the interception of the straight line with the voltage axis(at $1/C^2$ =0) , represent the built in potential (V_{bi}) as shown in fig(3).

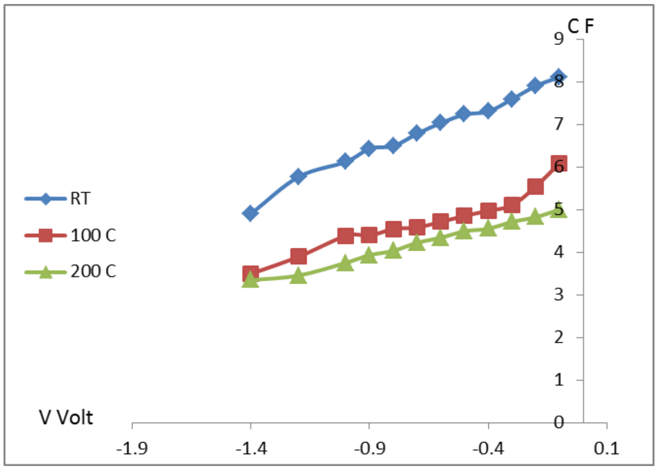


Figure 2: variation of Capacitance versus reverse bias voltage for a-Ge:Sb/c-GaAs hetrojunction at different T_a.

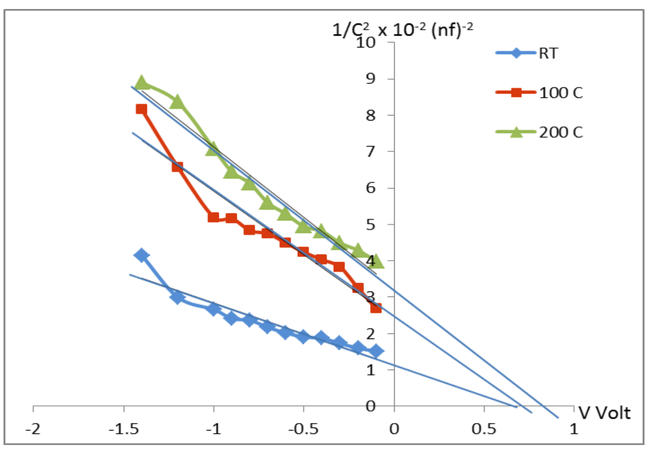


Figure 3: variation of $1/C^2$ versus reverse bias voltage for a-Ge:Sb/c-GaAs hetrojunction at different T_a.

Table 1: The calculated values of V_{bi}.

$T_a{}^0C$	V_{bi} Volt
RT	0.645
100	0.71
200	0.84

We can see from table (1) and fig(3) the variation of Vbi from (0.645 to 0.84)Volt when annealing temperature change from (RT to 200)^{0}C . This variation may be due to the improvement in the structure of the film. These results are almost conform with Akram Norri [7].

Fig(4) shows I-V characteristic for a-Ge:Sb/c-GaAs hetrojunction at forward and reverse bias voltage (-1.8 - 2.2) volt for different annealing temperature(RT, 100, 200)^{0}C.

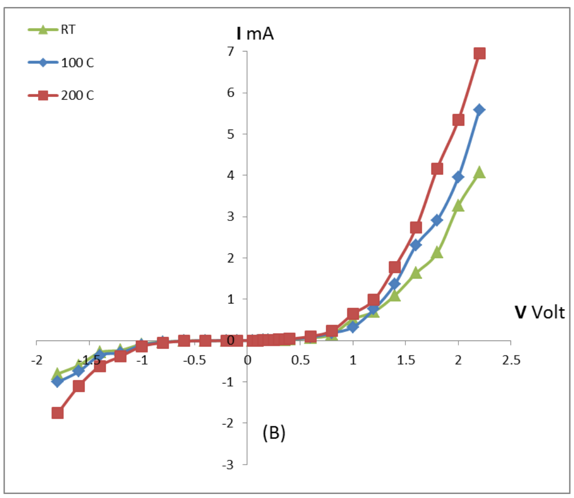


Figure 4: illustrate how the current voltage characteristic in the dark appear at different annealing temperature (Ta).

We observed that the current increases slightly with increasing of annealing temperature because the increasing of temperatures causes a rearrangement of the interface atoms and reduce the dangling bond, surface states and dislocation at interface layer between a-Ge:Sb and c-GaAs which leads to improvement of the junction characteristics. These results are conform with Sahni et al. [8] and Teleman et al. [9].

Another important features are observed in the fig(4), the saturation current(I_s) can be calculated from intercepting the straight line with the current axis at zero voltage bias.

The variations of saturation current (I_s) and identity factor (β) with different annealing temperature are shown in table (2). This data indicates that the value of the saturation current decreases with increasing annealing temperature.

This behavior attributed to the improvement of crystal structure at interface layer, also the reduction of dangling bonds as well as the density of state in a-Ge:Sb.

Table 2: The saturation current (I_s) and ideality factor.

Ta^0C	I_s mA x 10^{-5}	β
RT	5.8	2.641
100	3.9	2.52
200	2	2.358

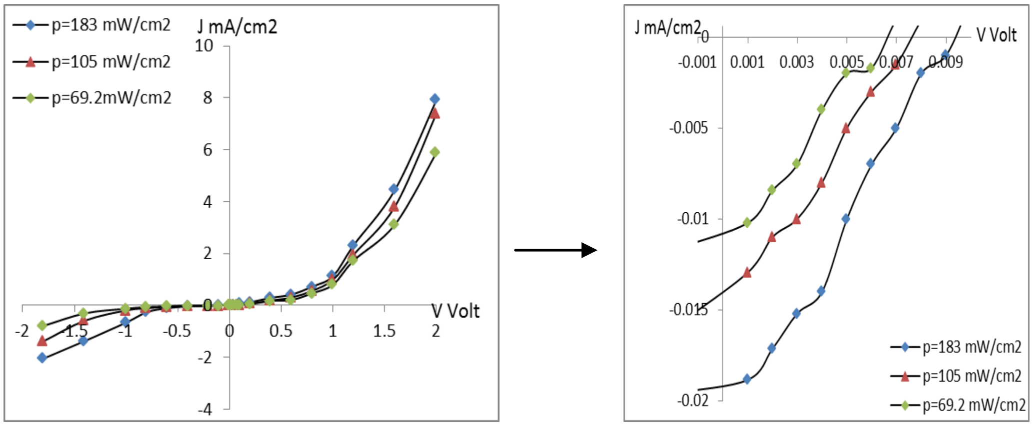
In another attempt we have studied the relation between the photocurrent density (Jph) and bias voltage of the a-Ge:Sb/c-GaAs diodes at different annealing temperature fig(5). The measurement were carried out under different incident power density equal to (0, 69.2, 105, 183)mW/cm^2.

All samples show a photocurrent density increases with increasing of the bias voltage and annealing temperature, this may be attributed to the increasing in the grain size and reducing the grain boundaries and improvement of structure which leads to increase of the mobility and photocurrent density. In general through looking at figs(5) we can notice that the short circuit current density(J_{sc}) occurs when v=0,while the open circuit voltage (v_{oc}) occurs when the net total current equal to zero. This parameter is very important because it can determine the region on which the hetrojunction operators onit, and it can separate the generated pairs without the need to apply any external field.

We can observe from fig(6) that the J_{cs} increases with increasing incident power intensity and annealing temperature.

The behavior of J_{sc} is linear at the first section and this attributed to the incident power intensity.

In second section there is a tendency to saturation with increasing of the incident power intensity at limited range, due to the recombination effect ;as well as we can see fig(7) the V_{oc} increases with increasing of incident power and annealing temperature due to the reduction in density of interface state. This result is in agreement with Ismail et al. [10].



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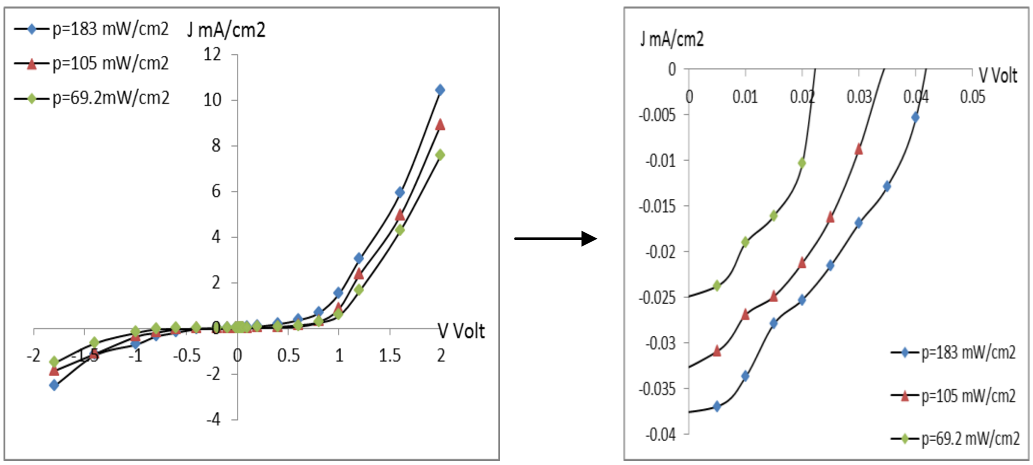
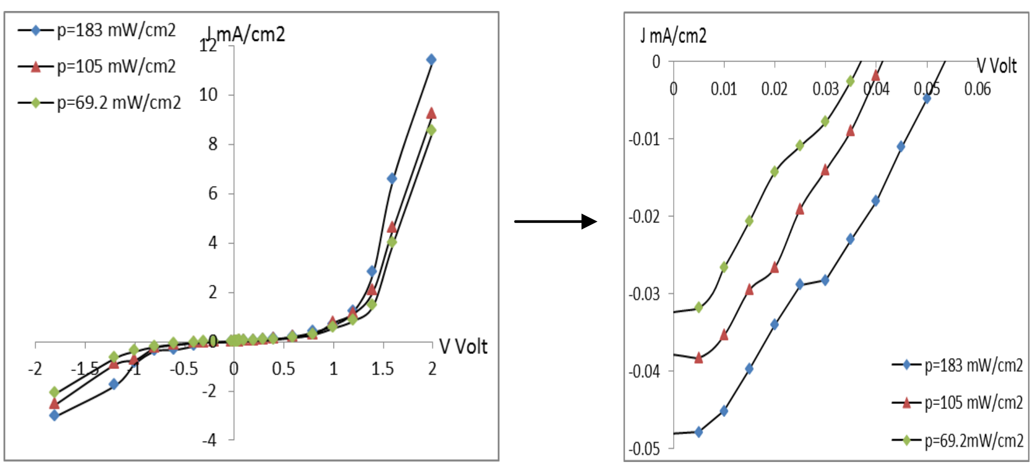


$T_a = 100^0C$



$T_a = 200^0C$

Figure 5: I-V characteristics under illumination for a-Ge:Sb/c-GaAs heterojunction for thickness of 0.5 μm at different annealing temperatures

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