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Microstructural and Electrical Characterization of Pt/Si Nanowires Schottky Diode Grown by Metal Assisted Chemical Etching Method

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Abstract: In this report, microstructural and electrical parameters have been evaluated for Pt/Si nanowires Schottky nanocontact, grown by metal-assisted chemical etching method. Schottky contact has been formed by placing a platinum conducting tip of STM at an optimized distance (in Armstrong) from the peak of SiNWs. At an optimized separation between the tip and silicon nanowires, resulting I-V characteristic shows it rectifying behaviour. Ideality factor has been evaluated as 3.7 and reverse breakdown voltage is -5V.

Keywords: Silicon Nanowires (SiNWs), Schottky contact, platinum tip

1 Introduction

With the advancement of technology in the field of semiconductor, nanominiaturization has emerged out to be the requirement for the growth of electronic industry. Among several nanoelectronic devices, Nanowires emerged as a promising candidate for electronics and optical devices [1]. Nanowires can be characterized by their high aspect ratio i.e. length to diameter ratio [2]. Nanowires can be used to fabricate various electronic devices i.e. sensors, diodes etc. It is noteworthy here that due to faster switching speed and lower cut in voltage of Schottky diode, they are suitable for majority of electronic applications. Schottky diode is basically a metal semiconductor junction showing improved rectifying property [3]. However growth of metal semiconductor nanowire junction is still a vital issue that needs to address. Another interesting property related to the Nanowires can be observed when silicon Nanowires are grown i.e. they show direct bandgap that can be made wider by decreasing the diameter of Nanowires. This property triggers the use of silicon Nanowires in optoelectronic devices.

In the present paper, Scanning tunnelling Microscopy (STM) is used to derive the I-V characteristic of Pt/SiNWs

Schottky nanocontact. STM is based on quantum tunnelling. When a conduction tip is brought near the surface, a bias voltage applied between the two that allow electron to tunnel through the vacuum between them. The resulting tunnelling current is a function of tip position and applied voltage [4]. Metal assisted chemical etching (MACE) method has been used to fabricate silicon Nanowires (SiNWs) [5]. In order to observe microstructural property SEM and AFM have been done that shows well aligned SiNWs growth on silicon substrate. For the present experiment, platinum tip was placed at an optimized distance from the substrate to characterize the I-V characteristic of Pt-SiNWs. Analysis was done in non contact mode to avoid manipulation of samples.

2 Experiment Detail

Metal assisted chemical etching (MACE) method has been adopted for the growth of SiNWs. Initially Si wafers were cut into 2*2 cm² pieces and subsequently cleaned with RCA-1 and RCA-2 cleaning methods at room temperature. Cleaned wafers were then dipped into the etching solution prepared by taking 10 ml of AgNO₃ (0.02M) and 10ml HF (5M). The etchant solution was stirred slowly for 1 min under room temperature before immersion of cleaned samples. Etching completes after 30

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min, and the samples were rinsed thoroughly with deionized water afterward for 3- 4 times. A thin layer of Ag nano particles were deposited on the wafer and then the samples were immersed in etchant solution composed of HF (5M) and H₂O₂(0.4M). This process was continued for half an hour in dark under room temperature. Further, HF treatment was given to remove any residual oxide layer. After this sample were cleaned with DI water and dried under N₂ flow. After the successful fabrication of SiNWs, STM has been used to derive the I-V characteristic curve of Pt-SiNWs nanocontact by using a Platinum coated conducting probe with sharp tip. The schematic of the arrangement has been shown in figure 1.

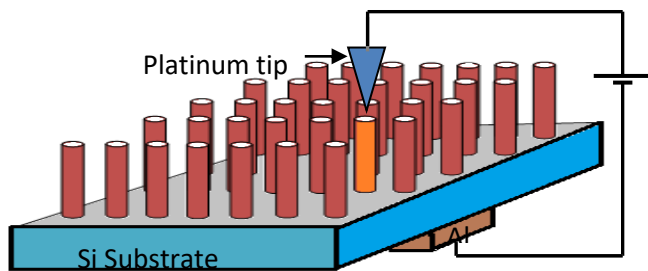


Figure 1. The schematic arrangement for STM measurement

3 Results And Discussion

3.1 Structural Analysis

The crystalline nature and structural properties of the as-grown SiNWS were measured by using X-ray diffractometer (XRD) [Rigaku Smartlab, with Cu-K α radiation ($\lambda=1.540568$ Å)]. Fig.2 shows the XRD diffraction pattern of the SiNWS. The XRD diffraction peaks were found at 56° corresponding to (311) planes in the SiNWS respectively. The crystallite size (D) of the SiNWS was obtained from the Debye-Scherrer equation (1) [6]

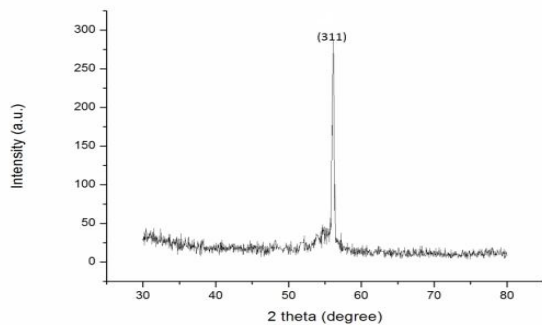


Figure 2. XRD Spectrum of SiNWs on p- Si substrate

$$D = \frac{0.9\lambda}{\beta \cos\theta} \quad (1)$$

where β is the full-width at half maximum (FWHM) and peaks are located towards an angle 2θ . All the parameters are listed in Table I. The strain in the SiNWs was obtained by the equation (2) [7].

$$\xi = \left[\frac{\lambda}{D \cos\theta} - \beta \right] \times \frac{1}{\tan\theta} \quad (2)$$

3.2 Surface Morphological Analysis

The surface topography and size of nanorods were characterized using a scanning electron microscopy (ZEISS EVO MA 15) as shown in fig.3. SEM images confirm the growth of well aligned SiNWs vertical to the p-Si substrate. Further the typical average height and diameter of the grown SiNWs has been observed to be 2 μ m and 100 μ m, respectively.

3.3 Surface Topographical Analysis

The roughness and morphology of the SiNWs have been further evaluated by using Agilent 5500 Atomic Force microscopy (AFM). The morphology of the SiNws array as shown in fig.4 was obtained in non contact mode by AFM using Si₃N₄ tip. Large diameter of nanowires is obtained by AFM as compared to diameter obtained by SEM because of tip convolution effect [8]. The grain size, average roughness (R_a), root mean square (rms) roughness (R_q) and total roughness (R_t) of the SiNWs were also calculated.

3.4 Electrical Analysis

I-V characteristics for the Pt- SiNWS Schottky nanocontact were measured using STM by placing the Pt Tip near the head of SiNWs as shown in fig. 1.

Through STM small area has been scanned to confirm the position of single nanowire and then Pt-tip was brought on the head of wire to form nanocontact. At an optimized separation tunnelling of carrier between Pt tip and SiNWs commence due to the induced electric field when bias voltage is applied, that results in reduction of Schottky barrier height. I-V measurement was performed in constant separation mode in which the tip – sample separation was established at 1.5 V with the tip at virtually ground. I-V curve has been obtained by scanning 30 times at single position.

The fabricated Schottky diode is forward biased for positive voltages and reverse biased for negative voltages. This property can be used to determine the type of majority

Table 1. Inter planar distance and crystal size value calculated from XRD data

SiNWs	2 θ	FWHM($^{\circ}$)	Crystallite Size (\AA)	Interplanar Spacing(\AA)	Strain
Catalyst free	56	0.244	384	1.639	8×10^{-3}

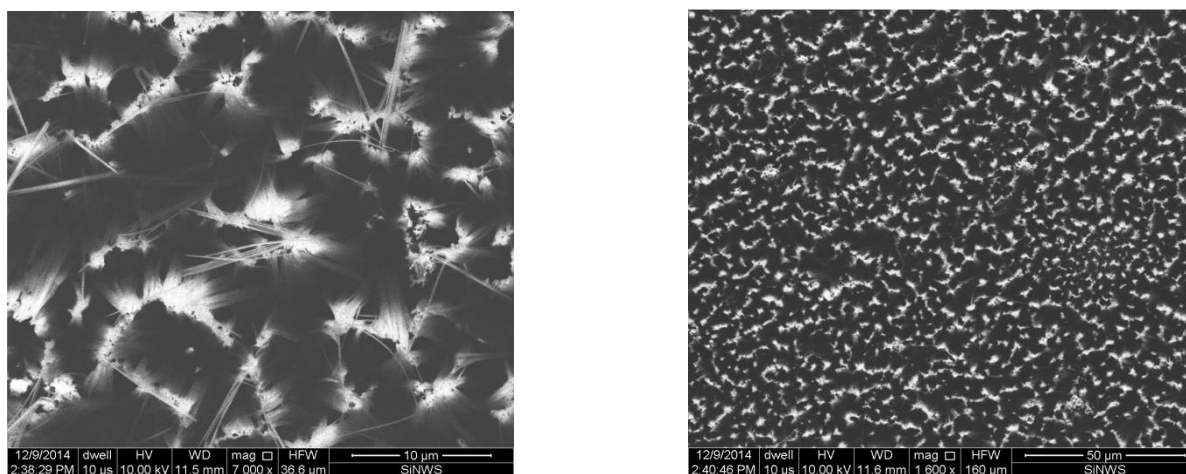


Figure 3. SEM image of the as-synthesized SiNWs grown on a Si substrate.

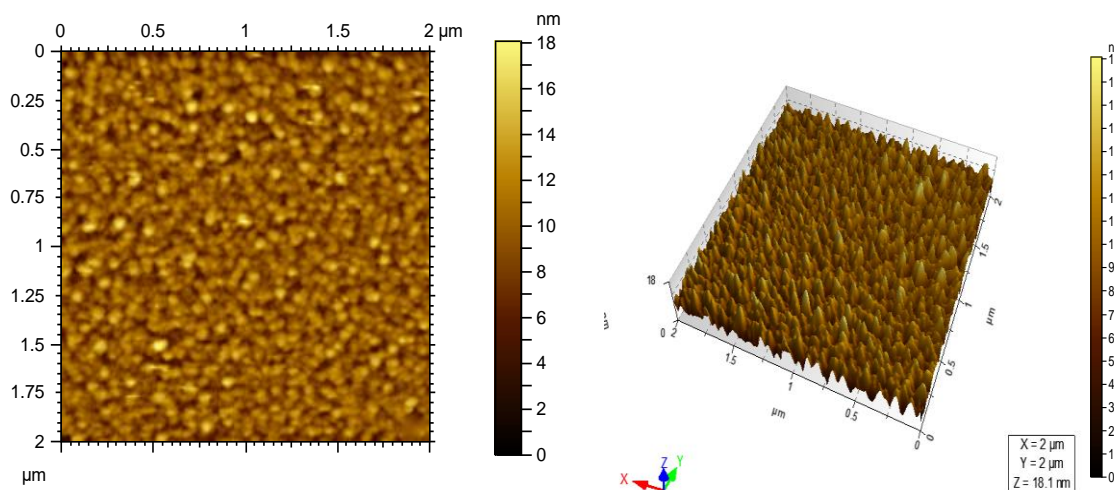


Figure 4. AFM image of the as grown SiNWs

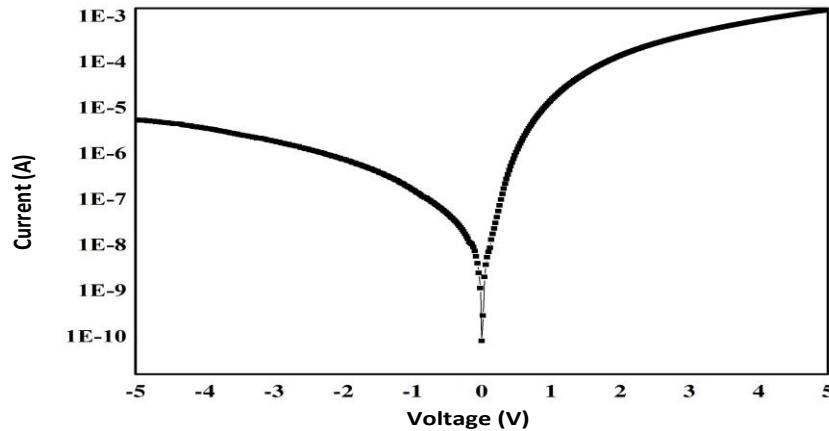


Figure 5. Current (I)-Voltage (V) characteristics of metal /SiNWs Schottky contacts.

From AFM results using picoimage software. All the parameters are listed in Table 2

Table 2. Roughness calculated from AFM data

Parameters	Value (nm)
grain size	38.5
average roughness (R_a)	2.59
root mean square (rms) roughness (R_q)	3.28
total roughness (R_t)	181

charge carrier from the rectifying behaviour of the Schottky contact [9]. We have seen so far that the properties of a metal-semiconductor contact are determined by the space-charge layer in the semiconductor. Due to the boundary conditions at the metal surface, the charges in the space charge layer will induce image charges in the metal. The interaction with these image charges effectively lowers the barrier height by an amount $\Delta\phi$. The current-voltage characteristic of a Schottky metal-semiconductor contact shows rectifying behaviour as shown in fig.5 (Pt has a high work function of 5.6 eV and Si has an electronic affinity of 3.9 eV [9]) with a rectification ratio of 4115 at +5 V. The

current across a Schottky diode and ideality factor (η) have been calculated using by thermionic emission theory [10].

$$I = I_0(e^{qV/\eta kT} - 1) \quad (3)$$

$$\eta = \frac{q}{kT} \frac{\Delta V}{\Delta \ln I} \quad (4)$$

where η is the ideality factor, k Boltzmann constant, and T is the absolute temperature. A is the Schottky contact area, A^* the effective Richardson constant (theoretically $A^*=32 \times 10^4 \text{ Am}^{-2} \text{ K}^{-2}$ [11]). The ideality factor (η) has been extracted from the slope of $\ln(I)$ - V plot is 3.7. The ideality factor (η) is in range 3-4 for Pt/SiNWs/n-Si/Al structures. The underlying cause for $n > 1$ can be attributed to either the existence of an interfacial layer, the barrier inhomogeneity, or the barrier height lowering due to the image-force which is voltage dependent [12]. The possible reasons may be attributed to the introduction of SiNWs and the different methods for the formation of thin Pt layer. A good Schottky contact results when a tip is placed at an optimized distance to the nanowires. Here, the contacts are in nano scale non contact mode, leading to a high electric field on the Silicon top surface beneath the contact point. Hence, the Schottky barrier thickness decreases, resulting in easier electron tunnelling across the M/SC interface and a large ideality factor [13].

4 Conclusions

SiNWs have been successfully grown on n-silicon (100)

substrate with the help of metal-assisted chemical etching (MACE) method. XRD, SEM, AFM and STM have been used to study the structural, morphological, topographical and electrical properties of SiNWs. It has been observed that SiNWs grown by etching have large crystallite size, small FWHM and less strain. The surface morphology study by SEM confirms the growth of symmetrical and vertically aligned Si NWs. The grain size and the roughness of the surface have also been evaluated. By placing the tip of Pt-coated STM probe on the head face of the SiNWs, a Pt-SiNWs diode has been formed. The I-V characteristics of pt/SiNW Schottky diode revealed rectifying properties in terms of rectification ratio and ideality factor of ~4115 and 3.7, respectively.

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