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A Regularly Modularized Multiplexer-based Full Adder for Arithmetic Applications

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Abstract: In this paper, we propose a novel multiplexer-based full adder design, denoted as MUXFA, by using regular modules for arithmetic applications. The MUXFA full adder is composed of three identical modules, in which each module separately operates for XOR-XNOR function, sum function, and carry function. The structure of the multiplexer-based full adder can be easily constructed by merely a single multiplexer module, its follows comes the features including fast design time, regular structure, simple layout, and enhanced layout efficiency. Furthermore, n-bit adder can be realized in regular architecture by using a single multiplexer module. The advantages of the design are with design simplicity, design regularity, and integrated-circuit (IC) layout modularity. These characteristics are useful and important in cell-based design especially for increase in IC layout efficiency. Due to the regularity and modularity, the proposed full adder is utilization of nineteen transistors only. Comparing with the open literatures, the transistor count is reduced 26.3% to 47.3% and power-delay-product (PDP) is reduced 48% to 122%. In 16-bit ripple carry adder (RCA) architecture, the proposed adder in power consumption, time delay, and PDP characteristics all are greatly improved, particularly in PDP is reduced about 27.5% to 69.0%. The experimental results show that the multiplexer-based MUXFA full adder is verified to be effective and practical.

Keywords: Full Adder, Multiplexer-based Logic, Arithmetic, Adder Design

1 Introduction

Due to rapid advances in electronic technology, electronics market is becoming more competitive, which results in consumer electronic products requiring even more stringently high quality. The design of consumer electronic products requires not only light weight and slim size, but also low power and fast time-to-market. Therefore, the integrated circuit (IC) designers have to consider more important issues such as chip area, power consumption, operation speed, circuit regularity, and so on. Due to these design issues relevant to the key competitive factors of electronic systems, IC designers and electronic design automation (EDA) vendor are very concerned about the development of effective methodologies to fetch smaller chip area design, lower power consumption, faster operation speed and more regular circuit structure.

The arithmetic circuit is the important core in electronic systems. If the arithmetic circuit has good characteristics, the overall performance of electronic systems will be improved dramatically. Obviously, the performance of the arithmetic circuit directly determines whether the electronic system in market is competitive. It is well known that full adder is the crucial building block used to design multiplier, microprocessor, digital signal processor (DSP), and other arithmetic related circuits. In addition, the full adder is also dominant in fast adder design. Therefore, to effectively design a full adder with smaller chip area, low power consumption, fast operation speed and regular circuit structure, are the common required for IC designers.

Since full adder plays an extremely important role in arithmetic related designs, many IC designers puts a lot of efforts on full adder circuit research. Consequently, there are many different types of full adders have been developed for a variety of different applications. These

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different types of full adders have different circuit structures and performance. Full adder designs have to make tradeoff among many features including lower power consumption, faster operating speed, reduced transistor count, full-swing output voltage and the output driving capability, depending on their applications to meet the needs of electronic systems.

One important kind of full adder designs focus on adopting minimum transistor count to save chip area [1,2,3,4,5]. These full adder designs with fewer transistors to save chip area does have excellent performance, however, due to MOS transistors reduced, these full adders have threshold voltage loss problem and poor output driving capability. Some full adders are designed to emphasize making up for threshold voltage loss to improve circuit performance [6,7,8]. These full-swing full adder designs insist on using fewer MOS transistors to reduce circuit complexity to go along with reduced power consumption and delay time. However, the full-swing full adders have no output driver in design leading to signal attenuation problems when they are connected in series to construct multi-bit adders. Therefore, many studies focus on gathering many features such as full-swing voltage, powerful output driving capability and good power delay product [9,10,11,12,13] in the meantime to boost the performance of full adder circuit design as a whole. However, the penalties have to pay for taking too many design issues into consideration are increased circuit complexity, larger chip area, difficult layout design, and increased transistor count. Therefore, how to design a full adder circuit with better performance and simpler structure is the main goal of full adder design field. In order to design a full adder with low circuit complexity, good circuit performance and the modularized structures, a multiplexer-based full adder is proposed in this study. The multiplexer-based full adder has not only regularly modularized structure, but also superior circuit performance.

The rest of this paper is organized as follows: In section 2, some previous works on full adder design are discussed. A novel multiplexer-based full adder design is presented in section 3. In section 4, we show the experimental results and make a discussion. Finally, a brief conclusion is given in section 5.

2 Previous Works on Full Adder Design

The full adder function is to sum two binary operands A, B and a carry input C_i, and then generate a sum output (S) and a carry output (C_o). There are two factors affecting the performance of a full adder design: one is the full adder logic architecture, and the other is the circuit design techniques to perform the logic architecture function. Therefore, the full adder design approach requires using different types of logic architecture and circuit design technique to improve the total performance.

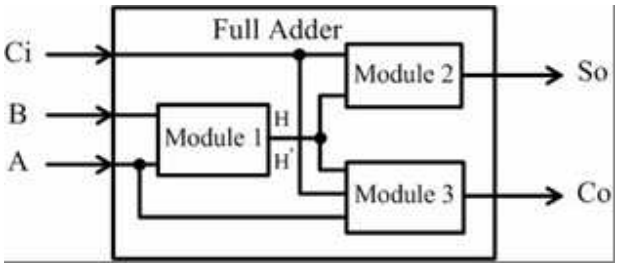


Fig. 1: Full adder logic architecture with three modules.

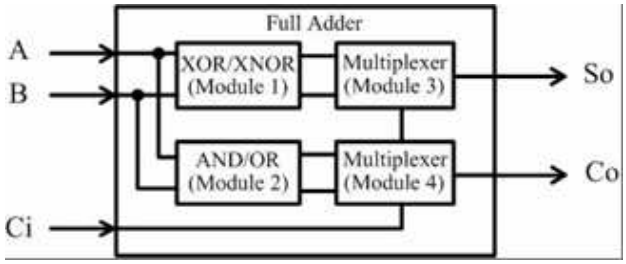


Fig. 2: Full adder logic architecture with four modules.

The traditional full adder logic architecture can be divided into three modules [6,7,8], and the logic architecture block diagram is shown in Fig. 1. New-HPSC full adder [9] and Hybrid-CMOS full adder [10] also belong to this category. These two full adders achieve logic functions of three modules by using pass transistor logic (PTL) and static complementary metal-oxide-semiconductor (CMOS) circuit design techniques.

Fig. 2 schematically show another logic architecture block diagram of a full adder in which logic architecture is divided into four modules. DPLFA full adder [13] and SR-CPL full adder [13] also belong to this category. DPLFA full adder and SR-CPL full adder achieve logic functions of full adder modules by using double pass transistor logic (DPL) and swing restored complementary pass-transistor logic (SR-CPL) circuit design techniques, respectively.

2.1 New-HPSC full adder

New-HPSC full adder [9], as shown in Fig. 3, is designed by using pass transistor logic and static CMOS circuit design techniques. New-HPSC adder logic architecture consists of three circuit modules including the XOR-XNOR module, sum module and carry module. The XOR-XNOR module in New-HPSC adder, designed by pass transistor logic circuit design technique, receives both inputs A and B to simultaneously produce two complementary output signals, i.e., XOR and XNOR

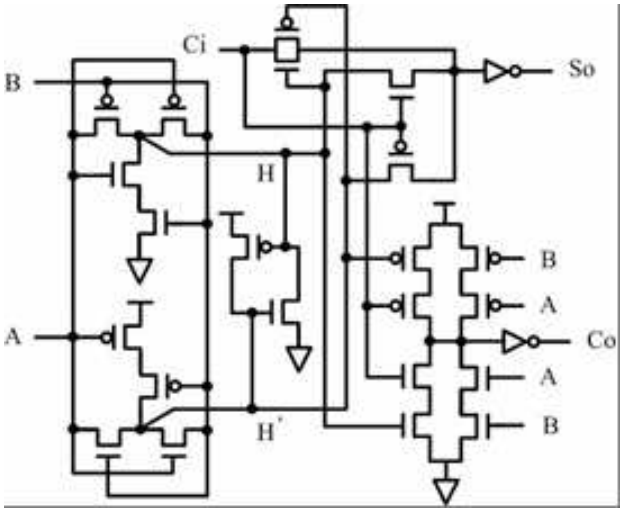


Fig. 3: New-HPSC full adder [9].

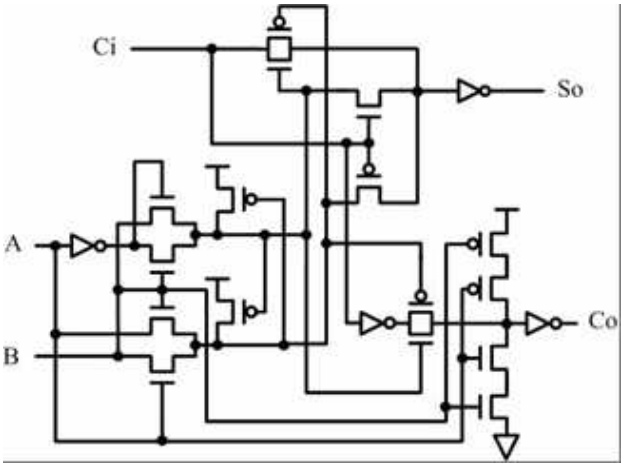


Fig. 4: Hybrid-CMOS full adder [10].

functions for *A* and *B*. Then the XOR and XNOR output signals drive sum module and carry module, to generate the sum output signal *S* and the carry output signal C_o. The carry module in New-HPSC adder is designed by static CMOS circuit design technique in order to reduce power consumption, increase operation speed and enhance output driving capability. The transistor count of New-HPSC adder is twenty-six to be larger due to fetch the prescribed features.

2.2 Hybrid-CMOS full adder

Based on both pass transistor logic and static CMOS circuit design techniques, Hybrid-CMOS full adder [10] is implemented as shown in Fig. 4. Hybrid-CMOS full adder is composed of three logic architecture modules including XOR-XNOR module, sum module and carry module. To make use of pass transistor logic circuit design techniques, Hybrid-CMOS full adder can produce both the XOR and XNOR signals at the same time by using only eight MOS transistors. The XOR-XNOR module performs XOR and XNOR operations on input A and B, and then both the XOR and XNOR output signals are used to drive sum and carry modules to produce the sum output *S* and carry output C_o. By using static CMOS circuit design techniques, the carry module of the Hybrid-CMOS full adder can achieve enhanced performance and high driving capability. Due to adopting both the new XOR-XNOR module and carry module, the transistor count of Hybrid-CMOS full adder can reduce to twenty-four. As a result, the circuit complexity of Hybrid-CMOS full adder is simplified and chip area as well.

2.3 DPLFA full adder

Fig. 5 schematically shows the DPLFA full adder [13] which is designed by using double pass-transistor logic circuit design technique. The logic architecture of DPLFA full adder has four modules in which module 1 denoted as XOR-XNOR module, module 2 denoted as AND-OR module, module 3 denoted as multiplexer module, and module 4 also denoted as multiplexer one. The XOR-XNOR module, designed by using double pass transistor logic circuit design technique, is together with the multiplexer module (module 3) to perform the sum operation for DPLFA full adder. The AND-OR module, constructed of powerless AND gate and groundless OR gate, is matched with the multiplexer module (module 4) to produce carry output signal C_o. In both multiplexer modules (module 3 and module 4), the carry input signal C_i is used as select-signal. Since possessing sum generation circuit and carry generation circuit separately, DPLFA full adder can enhance the total operation speed. However, the DPLFA full adder design requires twenty-eight MOS transistors, and thus increases circuit complexity relatively.

2.4 SR-CPL full adder

The SR-CPL full adder [13], depicted in Fig. 6, is designed by using the swing restored complementary pass-transistor logic circuit design technique. The logic architecture of SR-CPL full adder, same as that of DPLFA full adder, can also be divided into four modules. Module 1, denoted as XOR-XNOR module, is designed by using swing restored complementary pass-transistor logic technology to perform both XOR and XNOR logic operations as inputs *A* and *B* occurring. The XOR and XNOR output signals are then sent to the following

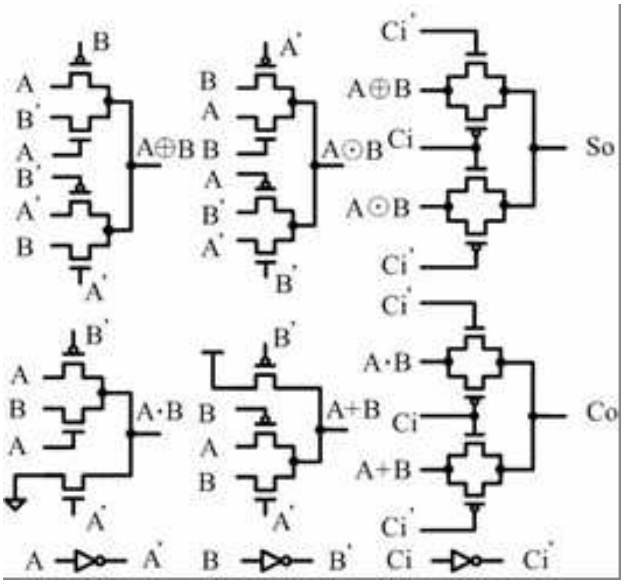


Fig. 5: DPLFA full adder [13].

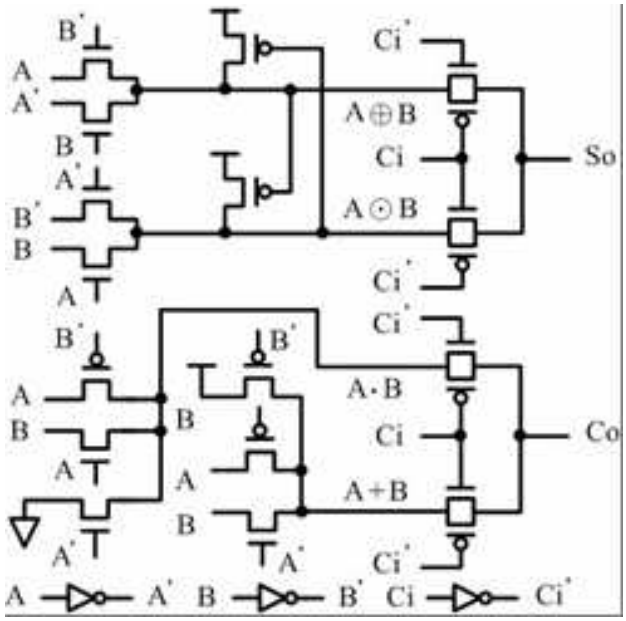


Fig. 6: SR-CPL full adder [13].

multiplexer of module 3 where C_i selects these signals to generate sum output S. In the case of $C_i = 1$, XNOR signal is selected and sent to the sum output; and if $C_i = 0$, XOR signal is selected and sent to sum output. Module 2 is the AND-OR module which consists of the powerless AND gate and groundless OR gate. Both these AND and OR output signals are then sent to the following multiplexer of module 4 in which C_i is used as select-signal to produce carry output C_o. In case of $C_i = 1$, OR signal is selected and sent to the carry output; and if $C_i = 0$, AND signal is selected and sent to the carry output C_o. Since SR-CPL full adder is constructed of individual sum generation circuit and carry generation circuit, the delay time of this one will be effectively reduced. However, the SR-CPL full adder requires twenty-six MOS transistors to design, which means its circuit complexity relatively increased.

3 Multiplexer-Based Full Adder Design

3.1 Energy restored multiplexer

Full adder is the crucial core to build the arithmetic unit. In order to pursue a more simplified circuit structure and better circuit performance, a novel multiplexer-based full adder, denoted as MUXFA, is proposed based on energy restored multiplexer. Energy restored multiplexer, denoted as ERMUX, consists of two NMOS transistors, a PMOS transistor and an inverter. Fig. 7 schematically shows the circuit structure of ERMUX. Notice that ERMUX possesses complementary select-signals X and X', and complementary outputs Y and Y'. ERMUX circuit

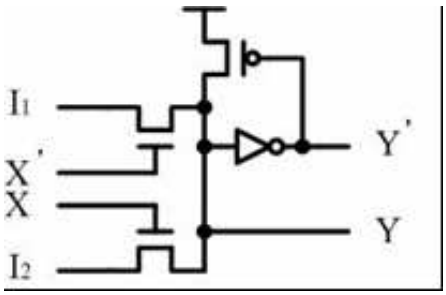


Fig. 7: Energy restored multiplexer.

structure is very simple since merely two NMOS transistors dominating its multiplexer function. However, when anyone NMOS transistor passes logic 1 signal, the output Y shows a weak-one state. In order to modify the weak Y output, a PMOS pull-up transistor in accompany with an inverter is used to pull the weak-one up to strong-one (i.e., Vdd-level) state. In case of $Y = 1$, ERMUX multiplexer reversed-phase output $Y' = 0$ will turn on the PMOS transistor so that weak-one Y output is pulled up to restore the energy to strong-one. Therefore, ERMUX possesses the full-swing node voltage. The Boolean functions for the complementary output Y and Y' are shown in Eqs. (1) and (2), respectively.

$$Y = I_1 X' + I_2 X, \tag{1}$$

$$Y' = \left(I_1 X' + I_2 X\right)', \tag{2}$$

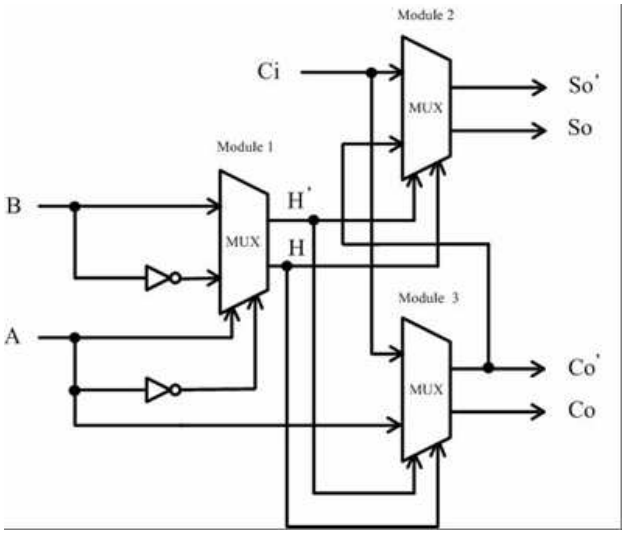


Fig. 8: MUXFA full adder block diagram.

3.2 Multiplexer-based full adder

A novel multiplexer-based full adder, denoted as MUXFA and shown in Fig. 8, is proposed by using ERMUX. MUXFA consists of three modules. Module 1, denoted as XOR-XNOR module, is the XOR and XNOR generating circuit. Module 2 is called sum module to perform the sum operation. And module 3 is denoted as carry module to produce a carry output. In spite of the full adder logic architecture with three modules similar to some previous works, proposed MUXFA has unique feature in performing three different functions for corresponding modules by using merely one ERMUX circuit. Obviously, the first emerged advantages of the MUXFA design are regularly modularized architecture and simplified layout complexity.

Fig. 9(a) shows the switch-level XOR-XNOR module where XOR and XNOR logic functions are realized by ERMUX. In XOR-XNOR module, B and B' are the data inputs, while A and A' are used as the select-signal inputs, to generate XOR output signal $H = A \oplus B$ and XNOR output signal $H' = A \odot B$. MUXFA then uses H and H' to drive the subsequent sum module and carry module to complete MUXFA full adder function. The sum module is shown in Fig. 9(b) in switch level. In sum module, ERMUX uses the carry input C_i and complement carry output C_o' as data inputs, and the H and H' as select-signal inputs, to produce the sum output S. In case of $H = 1$, then $S = Co'$; and if $H = 0$, then $S = C_i$. The sum output S is generated depending on sum module entirely implemented by merely the ERMUX multiplexer. Fig. 9(c) is the schematic of carry module. In carry module, ERMUX uses A and C_i as data inputs, while the H and H' are the select-signal inputs, to generate the output signal C_o. In case of $H = 1$, then $C_o = C_i$; and if $H = 0$, then

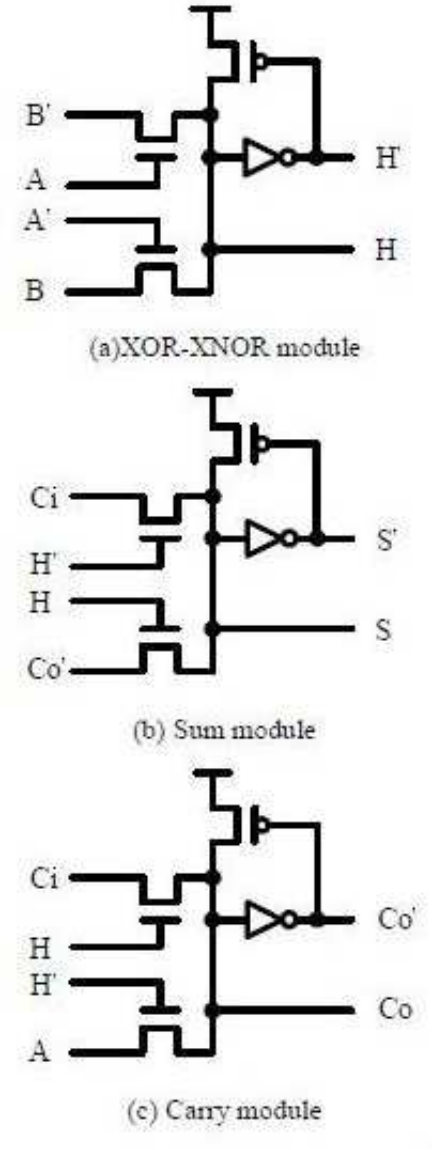


Fig. 9: Regularly modularized MUXFA full adder modules.

$C_o = A$. Thus, the propagation of carry signal from C_i to C_o requires the delay time for passing only an NMOS transistor. Therefore, another important advantage of MUXFA full adder is very fast carry propagation that also means high operation speed.

The sum output S and carry output C_o Boolean functions of MUXFA full adder are shown in Eqs. (3) and (4) below. The detail switch-level schematic of MUXFA is shown in Fig. 10, and the layout view of MUXFA full adder is shown in Fig. 11. Obviously, the proposed MUXFA full adder uses a single multiplexer ERMUX module to implement three different functional modules,

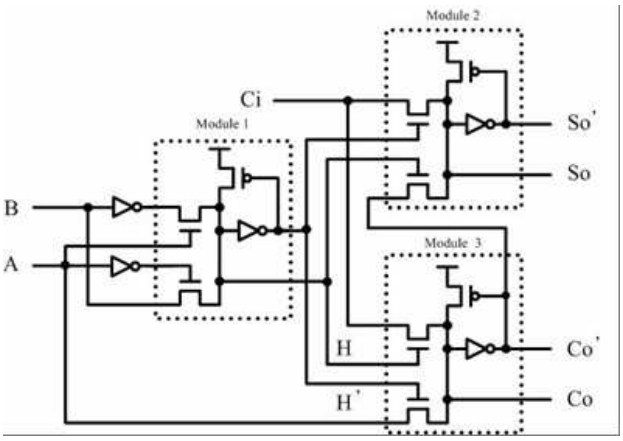


Fig. 10: MUXFA full adder schematic diagram.

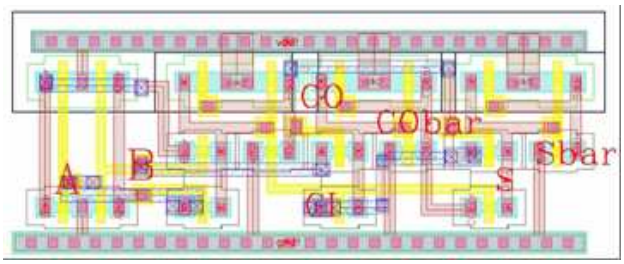


Fig. 11: MUXFA full adder layout view.

so that the full adder design can be fully regularly modularized to help improve the design efficiency.

$$S = H'C_i + HC'_o, \tag{3}$$

$$C_o = HC_i + H'A, \tag{4}$$

where $H = A \oplus B$, $H' = A \odot B$.

4 Experimental Results and Discussion

Based on TSMC $0.18-\mu m$ CMOS process technology and with the power supply voltage Vdd equal to 1.8V, the proposed multiplexer-based MUXFA full adder is compared with four previous designs New-HPSC, Hybrid-CMOS, DPLFA and SR-CPL. For a fair performance comparison, all full adders are composed of the same size of transistors, and experimented under the same simulation environment. The simulation environment is shown in Fig. 12. Circuit simulation will be experimented for 1-bit full adder and 16-bit ripple carry adder (RCA). The simulation issues include power consumption (Pd), the circuit delay time (Td) and power-delay product (PDP). In order to evaluate the

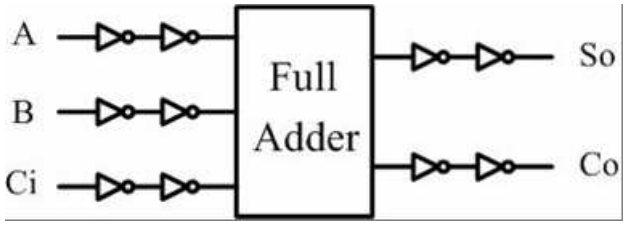


Fig. 12: Simulation environment diagram for full adder.

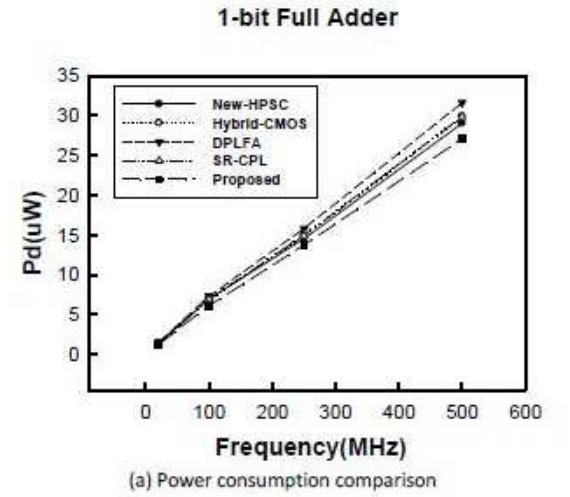
performance of full adders as operating in different frequencies, we will analyze and compare power consumption, delay time and power delay product in the frequency of $20MHz$, $100MHz$, $250MHz$ and $500MHz$.

The 1-bit full adder simulation results at frequency of $100MHz$ are shown in Table 1, where we can see that the transistor count (denoted as Tr. #) of MUXFA full adder can reduce about 26.3% to 47.3% when compared with other referenced full adders. In the operating frequency of $100MHz$, MUXFA can save 13.0% to 19.2% of power consumption, reduce 31.3% to 95.4% of delay time, and conserve 48% up to 122% of power-delay product when compared with other full adders. Fig. 13 shows the circuit performance comparison chart for a 1-bit full adder in the frequency of $20MHz$, $100MHz$, $250MHz$ and $500MHz$. According to experimental data in Fig. 13, MUXFA has better performance in power consumption, delay time and power delay product, and performs excellently particularly in the power-delay product.

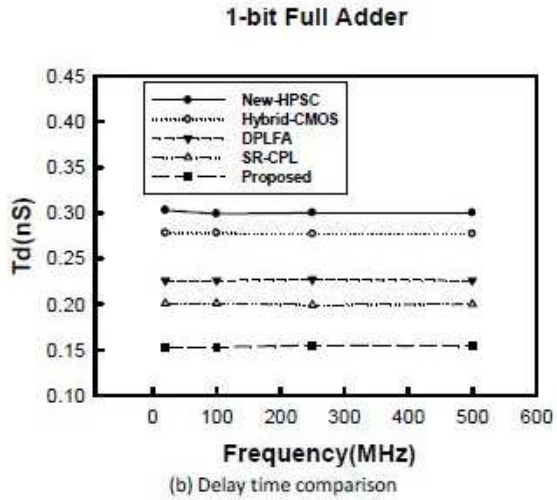
Table 1: Full adder simulation results at frequency of $100MHz$.

Full Adders	Tr.#	Pd(μW)	Td(nS)	PDP ($\mu W \times nS$)
New-HPSC [9]	26	6.951	0.299	2.078
Hybrid-CMOS [10]	24	6.907	0.278	1.920
DPLFA [13]	28	7.286	0.226	1.646
SR-CPL [13]	26	6.910	0.201	1.388
Proposed MUXFA	19	6.112	0.153	0.935

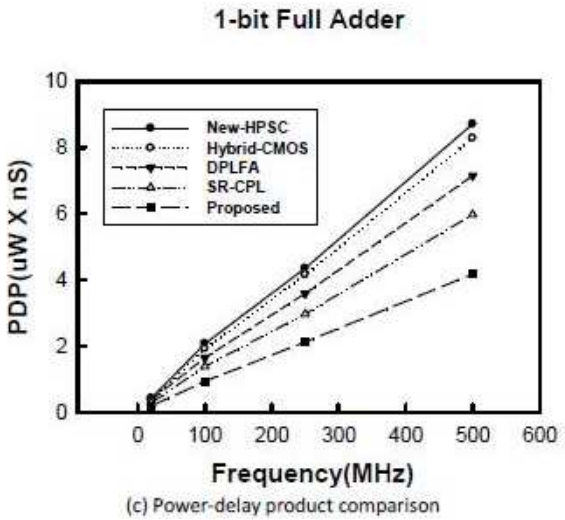
In order to evaluate the performance of full adders applied for arithmetic applications, all full adders are connected in series into 16-bit ripple carry adder. Table 2 is the simulation results for 16-bit RCA adders at frequency of $100MHz$, the 16-bit RCA adder composed of MUXFA can save 6.4% to 18.8% of power consumption, reduce 14.8% to 58.5% of delay time, and conserve about 27.5% to 69.0% of power-delay product when compared with other 16-bit RCA adders. Fig. 14 is the characteristics comparison chart for 16-bit RCA adder operating in different frequencies. Fig. 14 shows that MUXFA 16-bit RCA adder has better performance in



(a) Power consumption comparison

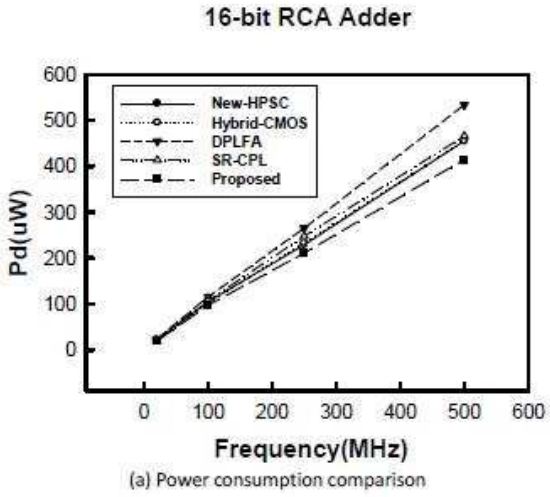


(b) Delay time comparison

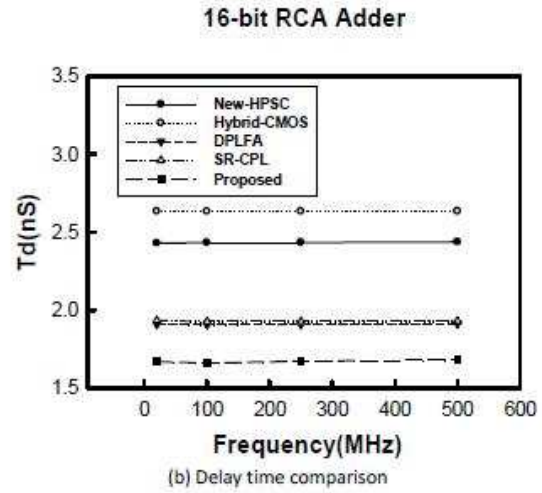


(c) Power-delay product comparison

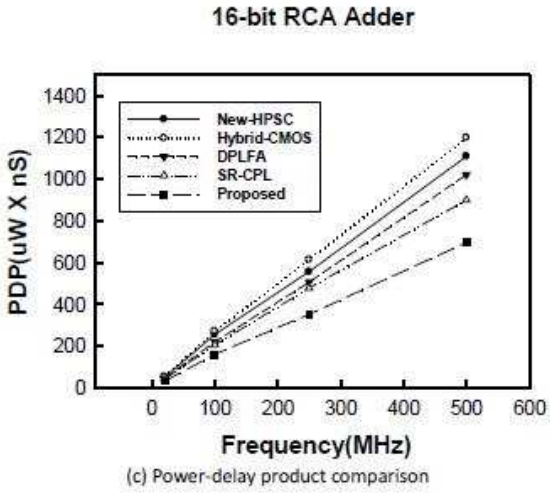
Fig. 13: Full adder comparisons at different operating frequencies.



(a) Power consumption comparison



(b) Delay time comparison



(c) Power-delay product comparison

Fig. 14: 16-bit RCA comparisons at different operating frequencies.

power consumption, circuit delay time and power delay product, even at different operating frequencies.

Table 2: 16-bit RCA simulation results at frequency of 100MHz.

16-bit RCA	Pd(μW)	Td(nS)	PDP($\mu W \times nS$)
New-HPSC [9]	105.3	2.432	256.0
Hybrid-CMOS [10]	103.5	2.632	272.4
DPLFA [13]	115.5	1.907	220.2
SR-CPL [13]	106.8	1.927	205.8
Proposed MUXFA	97.21	1.660	161.3

5 Conclusions

A regularly modularized multiplexer-based full adder, denoted as MUXFA, has been presented. In spite of three functional modules logic architecture similar to some previous designs, MUXFA completely implements the three functional modules by using merely the same energy restored multiplexer, i.e., ERMUX. The multiplexer-based MUXFA full adder can be easily constructed by using multiplexer ERMUX which makes the design simple and fast, and thus enhances the layout design efficiency. Due to the MUXFA full adder having regularly modularized circuit structure, it takes only nineteen MOS transistors to complete the design. Compared with New-HPSC, Hybrid-CMOS, DPLFA and SR-CPL full adders, the transistor count of MUXFA full adder can reduce 26.3% to 47.3%, which also means reducing both the silicon area and the manufacturing cost.

Based on the circuit performance at different frequencies, the multiplexer-based MUXFA full adder is found to be superior in power consumption, delay time and power delay product when compared with other four referenced full adders. At 100M Hz operating frequency, the MUXFA full adder can reduce 48% to 122% of power delay product. If the full adders are applied to construct 16-Bit RCA adders, the MUXFA 16-Bit RCA adder has the comparative advantage in power consumption, delay time and power delay product when compared with other four 16-Bit RCA adders. When operating at a frequency of 100MHz, the power delay product of MUXFA 16-Bit RCA adder can be reduced by 27.5% to 69%. Experimental results confirmed that the multiplexer-based MUXFA full adder design is effective and practical. When the MUXFA full adder applied to computer arithmetic circuits and consumer electronic systems, it will be able to improve design efficiency and also increase overall performance. Therefore, to apply MUXFA full adder in practical electronic products can enhance competitiveness in the market.

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