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Enhancing Radiation Performance of a 0.18 μm CMOS 60 GHz On-chip Double-Slot Vivaldi Antenna

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Abstract- This paper presents the design of a 60-GHz double-slot Vivaldi antenna (DSVA) using standard 0.18 μm CMOS technology. The antenna's two slots are uniformly excited in both amplitude and phase by a coplanar waveguide (CPW) power divider. A double-Y balun feeding structure is also used to transition from the CPW to the coplanar slot line (CPS). Two techniques are investigated to enhance the antenna's radiation characteristics. The first technique involves incorporating equal corrugations along the edges of the flare aperture, resulting in a significant gain enhancement of 0.9 dBi and an improvement in radiation efficiency by 7%. The second technique entails the construction of a planar arc reflector to suppress the back lobe, further enhancing gain by 0.7 dBi and radiation efficiency by 6%. The overall antenna dimensions are compact, measuring 870 μm \times 960 μm . It exhibits an end-fire radiation pattern with a simulated peak gain and radiation efficiency of +0.4 dBi and 38%, respectively. Furthermore, the measured reflection coefficient indicates that the impedance bandwidth of the DSVA spans from 50 to 70 GHz.

Keywords: Vivaldi antenna, 0.18 μm CMOS technology, Balun, CPW Power divider.

I. INTRODUCTION

The millimeter-wave band, especially the unlicensed 60 GHz band with a 7 GHz bandwidth (57-64 GHz), has recently become a significant research focus due to the rising congestion in the lower-frequency spectrum. This frequency band is highly suitable for high-speed, short-range communication. It is ideal for advanced applications such as 5G, the Internet of Things (IoT), and wireless personal area networks (WPANs) [1, 2]. Nevertheless, signals at 60 GHz are subject to substantial atmospheric absorption, restricting their transmission range [3].

On-chip antennas (AoCs) integrated into System-on-Chip (SoC) technology offer significant advantages, including miniaturization, cost reduction, low power consumption, and simplified packaging by eliminating lossy bond wires. However, they face challenges such as performance degradation due to the silicon substrate's low resistivity ($\sim 10 \Omega\cdot\text{cm}$) and high permittivity (11.9), which absorb electromagnetic waves and reduce efficiency. Additionally, mutual coupling in 5G applications can degrade performance, and accurate measurement is difficult due to integration with other on-chip components. Therefore,

innovative design solutions are required to fully harness the potential of AoCs [4, 5].

Numerous researchers have explored techniques to enhance AoCs' performance, including substrate post-processing methods such as micromachining and ion implantation to create high-resistivity substrates [6, 7]. While these techniques improve antenna radiation, they often reduce system-level integration and increase overall costs. Consequently, antennas must be fabricated using the standard CMOS process to ensure substrate compatibility and cost-effectiveness. Recent research focuses on utilizing various embedded reflecting surfaces, such as Artificial Magnetic Conductors (AMCs), to enhance AoC radiation [8-11]. AMCs electromagnetically shield the AoC from the lossy CMOS substrate due to their reflection characteristics. Although AMC layers can be implemented using the existing metal layers of the CMOS stack-up, making them cost-effective, AMC-based on-chip antennas typically have lower gains than other enhancement techniques.

Vivaldi antennas, a type of end-fire antenna, are gaining popularity in radar and array configurations due to their high gain, wide bandwidth, and simple structure [12]. However, the Tapered Slot Antenna (TSA), a type of Vivaldi antenna, faces a significant design trade-off. For better radiation characteristics, the TSA's width should be greater than $\lambda/2$, where λ is the wavelength. This requirement reduces the compactness of the antenna, which is crucial for practical applications such as MM-Wave imaging arrays. A few studies have proposed Vivaldi antennas on 0.18 μm CMOS technology, but many results have focused on Yagi antennas, examining their geometry, characteristics, and application-specific designs. Earlier 60-GHz Yagi and Vivaldi antenna designs employing CMOS technology have faced limited applications due to their low radiation efficiency, which typically ranges between 5% and 24% [5, 13-17].

This paper presents the design of a 60-GHz CMOS DSVA using 0.18- μm CMOS technology. The primary objective is to investigate techniques for enhancing radiation properties. Firstly, equal corrugations are etched on the edges to concentrate surface current towards the inner edge of the tapered slots, which enhances antenna gain and radiation efficiency. Secondly, a planar arc reflector is constructed to

reduce backside radiation, further improving antenna gain and radiation efficiency. Additionally, the double-slot structure ensures a more uniform distribution of the aperture field at the antenna's end, resulting in higher gain than a single-slot Vivaldi antenna (SSVA) of the same size. The paper is structured as follows: Section II provides details of the proposed 0.18 μm CMOS 60-GHz DSVA design, Section III presents the results and compares them with previous work, and Section IV offers the paper's conclusion.

II. ANTENNA DESIGN

The DSVA is designed using 0.18 μm CMOS technology with six metal layers (M1 to M6). The antenna without the arc reflector is located on the top metal layer (M6), while the ground plane is on the bottom layer (M1), minimizing conduction losses and enhancing performance. An arc reflector is also constructed between M1 and M6 using metal vias placed behind the antenna. The configuration of the proposed DSVA is depicted in Fig. 1. The antenna is designed on a 5 mm \times 5 mm substrate, a typical substrate area for a SoC. The tapered slots of the DSVA are created using two-slot lines in an exponentially tapered structure.

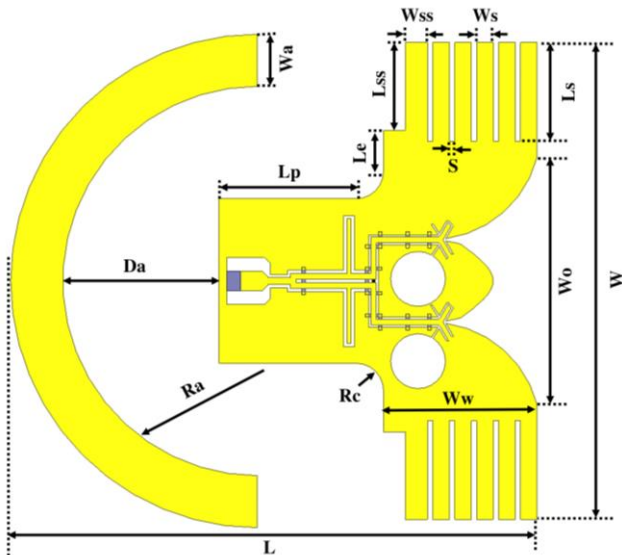


Fig. 1. Structure of the proposed DSVA.

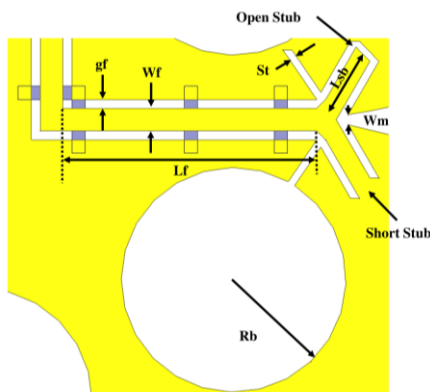


Fig. 2. Structure of the double-Y balun.

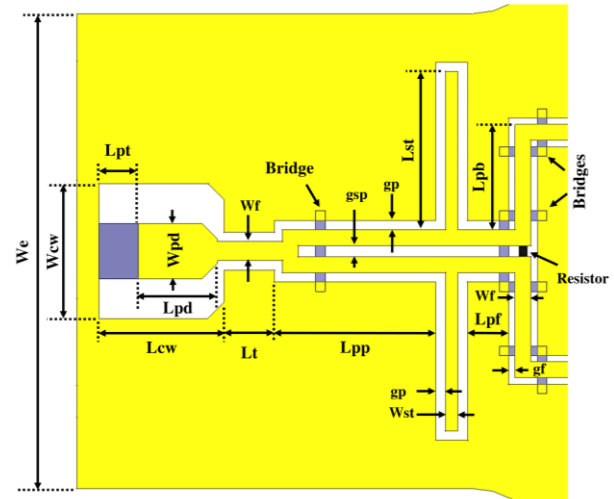


Fig. 3. Structure of the CPW power divider.

The CPW feeding technique connects the Ground Signal Ground (GSG) probe used in the measurement phase. This is achieved using CPW to CPS transitions to feed the antenna slots. A double-Y balun is a CPW to CPS transition that does not have any inherent bandwidth limitation [18]. Illustrated in Fig. 2, a double-Y balun, derived from a six-port double-Y junction, converts signals between balanced and unbalanced lines with minimal loss. Terminating specific ports with open and short circuits achieves the necessary antiphase reflection coefficients. The pad dimensions are designed to be 50 Ohms, and the input and output impedances of the double-Y balun are also chosen to be 50 Ohms. Additionally, a CPW power divider is employed to ensure that the two slots of the DSVA are excited in uniform amplitude and phase, as shown in Fig. 3 [19]. In the CPW power divider, the isolation resistor with a value of 100 Ohms prevents unwanted signal coupling between output ports, ensuring high isolation, minimizing signal distortion, and improving circuit performance. Besides, bridges in the CPW circuit maintain signal integrity by suppressing unwanted slot line mode propagation and ensuring cleaner signal transmission [20, 21].

The Vivaldi antenna is often preferred due to its wide operating bandwidth. However, as the frequency increases, various issues degrade its radiation characteristics. One significant problem is the unwanted radiation from currents traveling along the flare termination sections. This radiation leads to gain reduction, side lobes, and pattern distortion but can be suppressed by corrugating the termination sections. The corrugations are incorporated along the edges of the Vivaldi antenna's structure to address this problem [1, 22]. In the DSVA, these corrugations enhance radiation performance by introducing inductance and capacitance, altering the current distribution along the edges. The corrugation structure effectively acts as a high-impedance region, concentrating the surface current toward the inner edge of the tapered slots. This results in an improved front-

to-back ratio, reduced backward radiation, enhanced directivity, and a more focused radiation pattern in the end-fire direction, significantly improving gain across a wide frequency range. Additionally, the corrugations increase the antenna's effective length, making the DSVA more compact. Furthermore, a planar arc reflector is strategically placed behind the antenna along its axis. This reflector effectively suppresses the back lobe, significantly enhancing the antenna's radiation characteristics.

III. RESULTS AND DISCUSSION

In this study, electromagnetic (EM) simulations were conducted using the ANSYS High-Frequency Structure Simulator (HFSS®). As listed in Table I, the antenna parameters were optimized through parametric studies and optimization techniques.

A. Effect of antenna position on its performance

The performance of an AoC is significantly influenced by its position on the substrate [5, 17]. Antennas near the edge perform better than those at the center due to reduced substrate losses and better coupling with the surrounding air. When optimally positioned, the antenna benefits from a smaller lossy substrate area in front of it, enhancing radiation efficiency and gain. In contrast, a centrally located antenna may suffer from increased losses due to the larger substrate area it interacts with, leading to lower efficiency and gain. Therefore, the optimal position for the proposed DSVA on the substrate is position (2), as illustrated in Fig. 4. When the DSVA is shifted to the right or left along the substrate edge, it maintains its performance. However, the maximum radiation pattern is slightly deflected due to substrate asymmetry around the DSVA. The comparison of the optimal performance location (Position (2)) and the central location (Position (1)) is depicted in Fig. 5, Fig. 6, and Fig. 7. Both antennas achieve matching at the desired bandwidth around 60 GHz. The total realized gain and radiation efficiency at position (2) surpass those at position (1) across the operational frequency band. Specifically, at 60 GHz, the gain increases from -1.4 dBi to +0.4 dBi, and the radiation efficiency improves from 16.8 % to 38 %. Moreover, the front-to-back ratio decreases from 7.6 dB to 4.7 dB when the antenna is relocated from position (1) to position (2).

Table I: Optimized geometrical parameters of proposed DSVA

W	L	Wo	Ww	Ws	S	Wss	Lss	
870	960	450	280	210	30	10	40	
Le	Lp	Da	Ra	Wa	Rc	We	Wcw	Lpt
75	250	285	450	95	50	300	85	25
Lcw	Lpd	Wpd	Wf	Lt	Lpp	gp	gsp	Wst
79	50	35	12	32	148	6	7	8
Lst	Lpf	Lpb	gf	Lf	Rb	St	Lsb	Wm
100	26	66.5	4	113	50	3.7	29.9	4.5
Rb	Units: μm							
50								

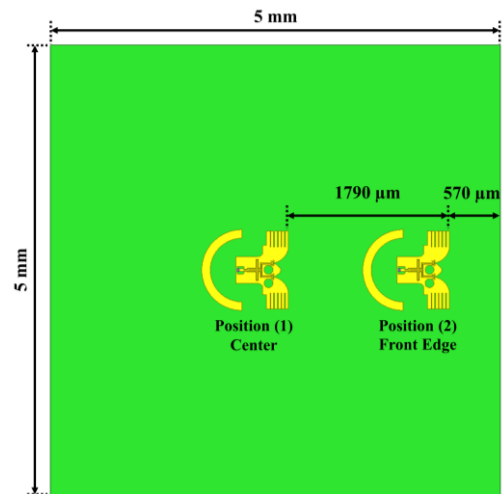


Fig. 4. Proposed DSVA design in Positions (1) and (2).

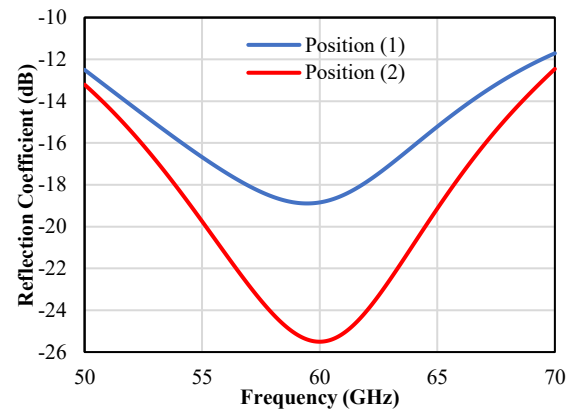


Fig. 5. Simulated reflection coefficient versus frequency for Position (1) and Position (2).

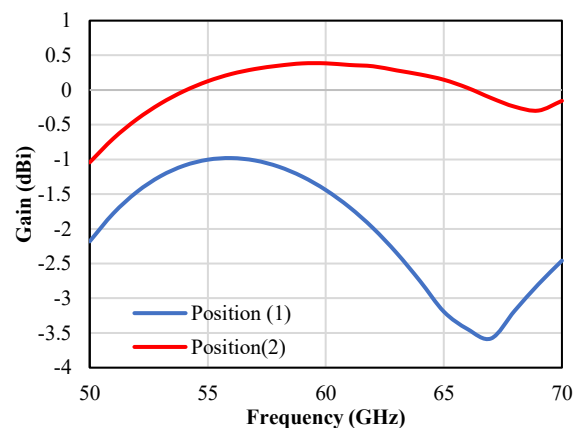


Fig. 6. Simulated gain versus frequency for Position (1) and Position (2).

B. Performance Enhancement Techniques

The effect of equal corrugations and planar arc on the proposed DSVA performance was studied at the optimum location (Position (2)). The antenna parameters were

adjusted to operate at the same center frequency of 60 GHz. The simulated curves of the reflection coefficient, the realized gain, and the efficiency are shown in Fig. 8, Fig. 9, and Fig. 10, respectively. For all configurations, the reflection coefficients are below -24 dB at 60 GHz. It can be observed that the effect of the equal rectangular corrugations is significant, resulting in a gain enhancement of 0.9 dBi and an improvement in radiation efficiency by 7 %. Furthermore, the planar arc reflector positively impacts the antenna's performance, improving the gain and radiation efficiency by 0.7 dBi and 6 %, respectively. As depicted in Fig. 8, the final design of the proposed DSVA operates at 60 GHz, covering a bandwidth of over 20 GHz, from 50 GHz to beyond 70 GHz. This indicates that the ultrawideband characteristic of the Vivaldi antenna is well-maintained after replacing the SSVA with the proposed DSVA. Due to the combined effects of both the corrugations and planar arc reflector, the gain and efficiency of the antenna are significantly increased in the end-fire direction to +0.4 dBi and 38 %, as shown in Fig. 9 and Fig. 10, respectively. The proposed DSVA also features compact dimensions, measuring $870 \mu\text{m} \times 960 \mu\text{m}$. Fig. 11 and Fig. 12 illustrate the simulated 2-D patterns in

the E- and H- planes and the simulated 3-D radiation pattern at 60 GHz for the final proposed DSVA design.

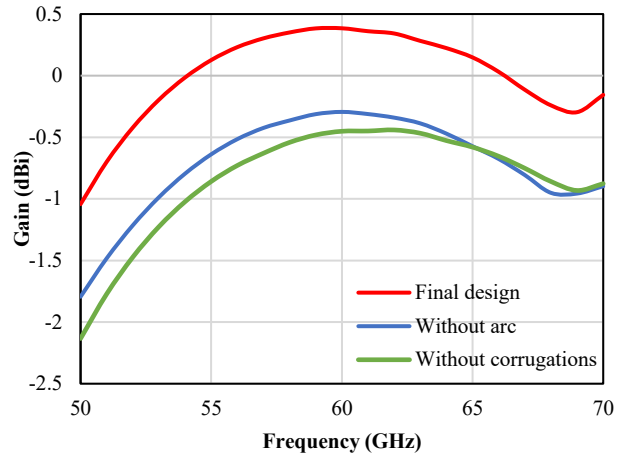


Fig. 9. Simulated gain versus frequency for DSVA.

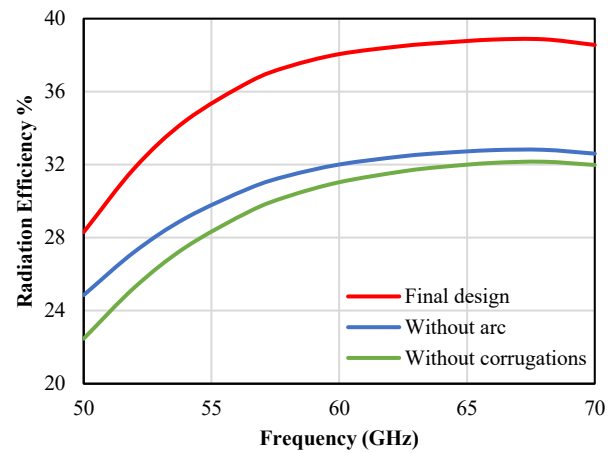


Fig. 10. Simulated radiation efficiency versus frequency for DSVA.

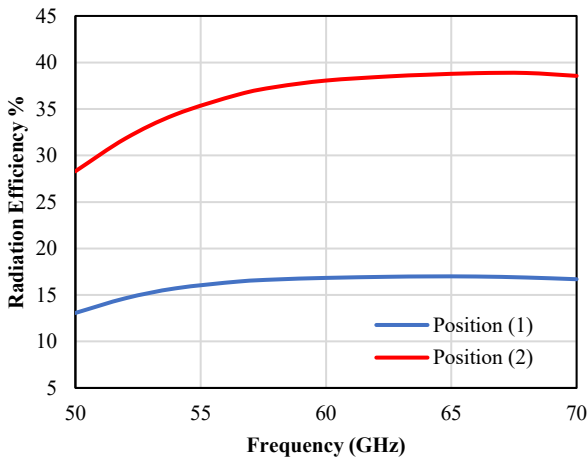


Fig. 7. Simulated radiation efficiency versus frequency for Position (1) and Position (2).

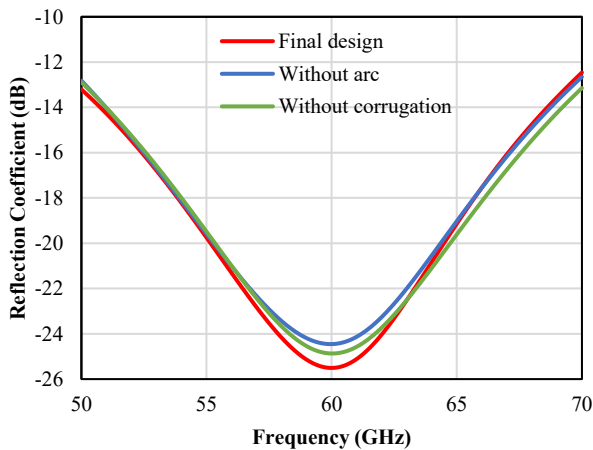


Fig. 8. Simulated reflection coefficient versus frequency for DSVA.

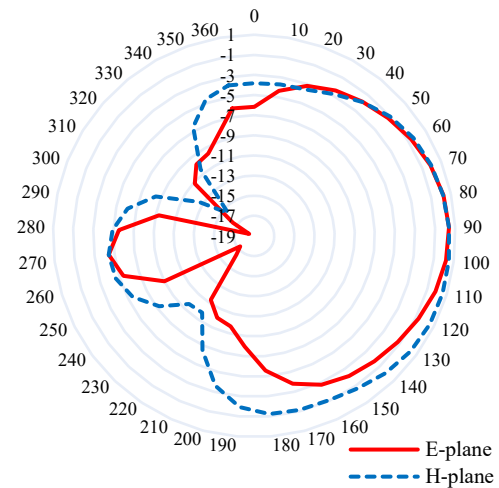


Fig. 11. Simulated 2-D patterns for DSVA at 60 GHz.

C. Measurement Results

The DSVA on-chip is fabricated using TSMC 0.18 μm CMOS technology. The photograph of the fabricated AoC is presented in Fig. 13. Measurements are conducted using an Agilent E8361C PNA, a manual probe station, and a Microtech 100 μm pitch Infinity® probe. A comparative analysis of the measured and simulated reflection coefficient parameters of the fabricated AoC on a 5 mm by 5 mm substrate is depicted in Fig. 14. The measured reflection coefficient results demonstrate matching within the 50 GHz to 67 GHz frequency range, corresponding to the maximum measurable frequency of the available PNA. The reflection coefficient measurements exhibit a wider bandwidth, indicating a lower quality factor. This broader bandwidth is attributed to additional losses not accounted for in the simulations.

Compared to the SSVA (with a size of 930 μm x 785 μm) proposed in [17], the DSVA can improve the performance better and in a wider band. The Simulated gain and efficiency for 60 GHz of the SSVA in [17] are -0.4 dBi and 32%, respectively, whereas those of the proposed DSVA in this paper are +0.4 dBi and 38%, respectively. Moreover, the DSVA's structure area is approximately the same as the SSVA in [17]. Finally, Table II presents a performance comparison of related on-chip CMOS DSVA designs. It shows that the proposed DSVA design has better performance and size than the recently reported on-chip CMOS antenna designs.

IV. CONCLUSION

A compact, high-performance 60 GHz DSVA using standard 0.18 μm CMOS technology has been designed and characterized. The antenna, measuring 870 μm x 960 μm , was optimized through simulations and fabricated for experimental validation. It significantly enhanced its radiation performance by incorporating key design features, including a CPW power divider, double-Y balun, corrugations along the flare edges, and a planar arc reflector. Simulation results demonstrated an end-fire radiation pattern with a peak gain of +0.4 dBi and a radiation efficiency of 38% at 60 GHz. Moreover, the measured impedance bandwidth extended from 50 to 70 GHz, confirming the antenna's wideband operation. The improvement in performance compared to SSVA is attributed to the double-slot structure, which creates a more uniform aperture field distribution, leading to higher gain. The proposed DSVA design outperforms previously reported on-chip 60 GHz antennas, making it a promising solution for compact, high-performance millimeter-wave.

Conflicts of Interest: The authors declare no conflict of interest.

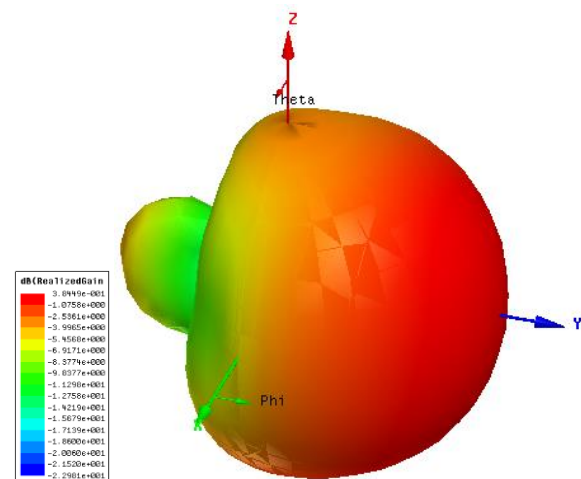


Fig. 12. Simulated 3-D pattern for DSVA at 60 GHz.

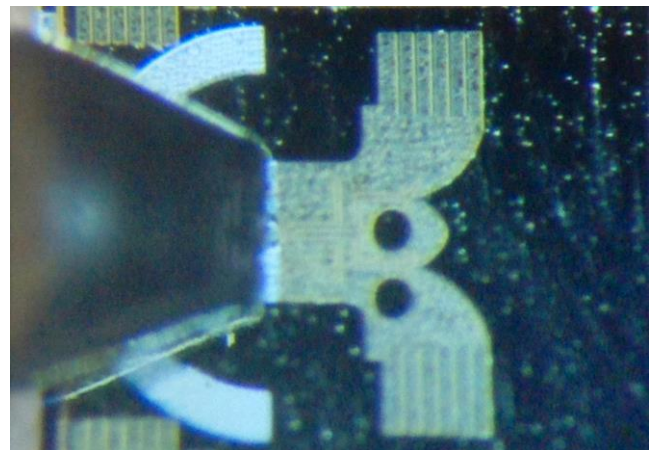


Fig. 13. Chip photo of the fabricated DSVA.

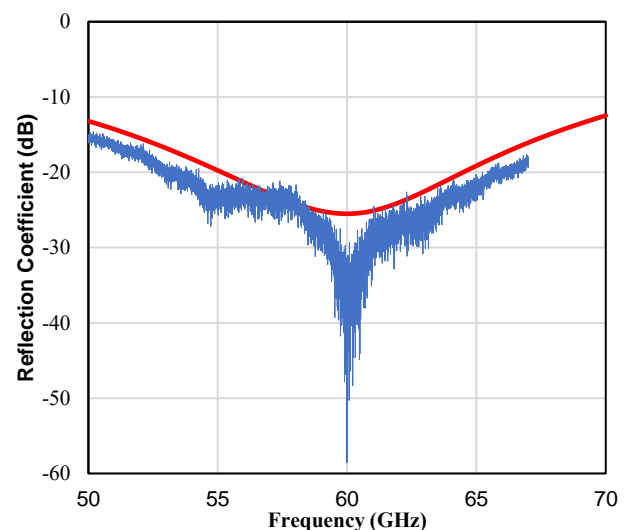


Fig. 14. Comparison between the simulated and measured reflection coefficient of the proposed DSVA.

Table II: Performance comparison of 0.18 μm CMOS DSVa with previously reported on-chip CMOS antennas.

Reference	Antenna Type	CMOS Process	Area (mm^2)	Frequency (GHz)	Gain (dBi)	Efficiency (%)
[16]	Vivaldi	0.18 μm	0.7×0.94	60	- 1.9 Simulated	24
[15]	Vivaldi	65 nm	1.73×1.75	60	- 3 Simulated	N/A
[17]	Vivaldi	0.18 μm	0.78×0.93	60	- 0.4 Simulated	32
[8]	Monopole	0.18 μm	1.2×1.2	60	- 2.64 Simulated	N/A
[23]	Monopole	Bi- CMOS	N/A	57	- 2.32 Simulated	21
[5]	Yagi	0.18 μm	1×0.87	60	- 0.74 Simulated	21.4
[24]	Triangular monopole	0.18 μm	1.2×1.2	64	- 0.4 Simulated	40.9
[9]	Slot monopole	0.18 μm	1.2×1.2	72	- 6.3 Simulated	22
[25]	Bowtie Slot	0.13 μm	1×1	84	- 0.58 Measured	N/A
[26]	Monopole	130 nm	0.36×0.19	85	- 0.35 Measured	N/A
[10]	Folded dipole	65 nm	4.7×2.87	94	- 1.4 Measured	60
[13]	Vivaldi	0.18 μm	1.2×1.2	100	- 4 Measured	17.7
This work	Vivaldi	0.18 μm	0.87×0.96	60	+ 0.4 Simulated	38 %

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