Applied Mathematics & Information Sciences
An International Journal

http://dx.doi.org/10.18576/amis/100620

Ultra High Voltage Device RESURF LDMOS Technology on Drain- and Source-Centric Design Optimization

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Received: 22 Jul. 2016, Revised: 15 Sep. 2016, Accepted: 22 Sep. 2016
Published online: 1 Nov. 2016

Abstract: We present drain and source-centric design optimizations of a linear P-top and dual-channel conduction path LDMOS (lateral double-diffused metal-oxide semiconductor) structure for low specific on-resistance (Ron.sp) powered transistor devices. The design was simulated using TCAD tools, and a real silicon device was fabricated successfully in accordance with the simulation. The 3D effect in the cylindrical layout with the linear P-top doping profiles was designed using an analytical model to obtain optimal charged balance for the drain- and source-centric regions. The silicon result, with an optimized P-top doping process window, achieved a breakdown voltage (BV) of 842 V, which was higher than 800 V. Thus, the use of a dual-channel conduction path technique with an N-top layer implanted over the P-top can improve Ron.sp by 25% without compromising BV.

Keywords: linear P-top, LDMOS, specific on-resistance, charged balance.

1 Introduction

We have previously fabricated a lateral double-diffused metal-oxide-semiconductor (LDMOS) device incorporated with a uniform n-drift region on a silicon substrate by using reduced surface field (RESURF) technology. Our device features increased breakdown voltage (BV) and lowered specific on-resistance (Ron.sp) [1] [2] [3]. In a single-RESURF device, the n-drift region must be fully depleted before the lateral electric field reaches a critical value, because the vertical depletion of the n-drift region is supported by a single junction. A double-RESURF device incorporates an additional layer of opposite conductivity (P-top layer) inside an extended n-drift region so that the total charge can be increased and the Ron.sp can be reduced. A double-RESURF technology utilizing a linearly varying doped (LVD) P-top layer was recently presented [4][5][6]. This layer can be fabricated using the optimal number of multiple P-type rings. Impurity dopants are implanted through a mask with a sequence of openings, and the device is subsequently annealed. The widths of the rings and the spacing between the rings must be optimized to achieve high BV. The N-drift region and the P-type multiple rings must be fully depleted to achieve double-RESURF functionality. The RESURF principle has been widely used to construct lateral high-voltage MOSFETs. The N-drift dose sensitivity, curvature sensitivity, and field oxide charge sensitivity must be optimized to obtain the desired BV and Ron.sp for the device. It is widely known, from the layout of race-track and multi-fingered LDMOS devices [5], that the curvature radius of the source or drain region affects the BV characteristic of a device [7]. As the radius of curvature decreases, the electric field lines show much greater crowding, indicating a higher local electric field. Hence, to achieve high BV, the LDMOS must have sufficiently large source-centric (SC) and drain-centric (DC) radii of curvature to avoid excessive electric field concentration. In such layouts, design rules tend to increase the chip area. The proposed low Ron.sp device, which uses the linear P-top double-RESURF technique and a dual-channel conduction path [8][9][10], is illustrated in Fig. 1. The DC and SC layouts are cylindrical; these cylindrical layouts were designed to achieve charge balance and stable BV in response to doping concentrations in the N-drift region. The device was laid out in a 2D/3D simulation, which was used to verify and further optimize the design before it was committed to silicon [7], [11]. The process was optimized using a simulation written in

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TSUPREM-4 to determine doping profiles. The device structure was simulated using MEDICI to verify the device concept and identify the electrical characteristics. The surface electric field had an almost flat distribution, unlike the parabolic distribution of a conventional lateral RESURF device. Experiments at Vg = 40V resulted in a Ron.sp of less than 145 m-cm^2 and a BV of 842 V for this linear P-top and dual-channel conduction path device.

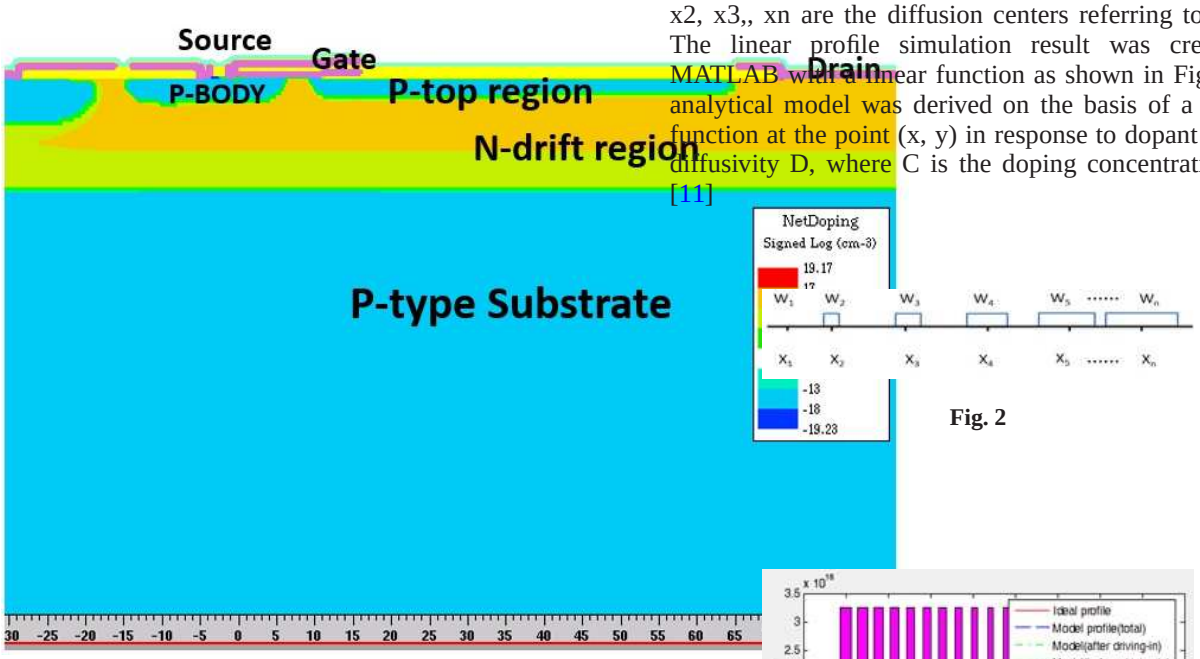

Fig. 1

etching processes. Subsequently, the poly-Si gate and source/drain (S/D) were implanted with arsenic, and the dopant was activated. Finally, the substrate contact patterning and the rest of the standard CMOS procedures were completed to fabricate this RESURF LDMOS device. Dopant diffusion was modeled and the results were used to make a linear profile for the P-top linear mask. Previous study shows the values used to define the slight width and spacing on the photo resist, where W1, W2,W3,,Wn are the widths of the mask openings and x1, x2, x3,, xn are the diffusion centers referring to Fig. 2. The linear profile simulation result was created in MATLAB with a linear function as shown in Fig. 3. An analytical model was derived on the basis of a Poisson function at the point (x, y) in response to dopant thermal diffusivity D, where C is the doping concentration. [7], [11]

Fig. 2

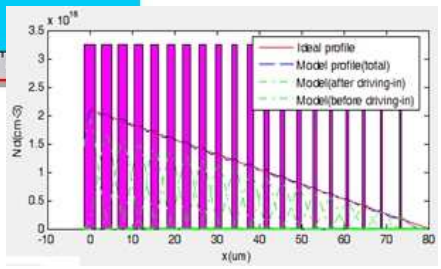

Fig. 3

2 Device Fabrication and Analytical Model

A linear P-top RESURF LDMOS with a dual-channel conduction path structure in its drift region was fabricated on a high-resistivity (100 ohm-cm) P-type Si wafer. An N-type epitaxial layer with a resistivity of 3 ohm-cm was grown to a thickness of 5 m. Subsequently the N-drift region was implanted, followed by high-temperature drive-in. Then, the linear P-top mask design, and optimized P-top and N-top dose were set to maintain the charge balance; the settings were known from the TCAD simulation. An extra conduction path of a lightly-doped N-top region with low energy was implanted over the P-top layer. A thick field oxide provided local oxidation of silicon isolation between the active regions of the device. Gate oxide was grown to a thickness of 90 nm in a furnace system. A 200-nm-thick poly-Si gate was deposited through low pressure chemical vapor deposition (LPCVD) and then defined using lithography and gate

$$dC(x,y,t)/dt = D[(^2C(x,y,z))/(x^2)+(^2C(x,y,z))/(y^2)] \quad (1)$$

$$C(t,x,y) = Q_s/(2Dt)[erf((x+W2)/(2Dt))-erf((x-W2)/(2Dt))]exp(-y^2/4D$$

The optimized model of P-top linear mask and profile can be defined by eq. (2). The process simulation parameters consist of the dose, temperature, diffusion time, and number of slit. A characteristic length is chosen based on the thermal budget and lithography limits, from which the number n for the mask windows is calculated for each P-top length. The linear P-top concentration profile simulated in TSUPREM-4 is shown in Fig. 4.

Relying only on our initial simulated results, we could fabricate our device successfully; the physical device yielded almost exactly the same results as the simulation

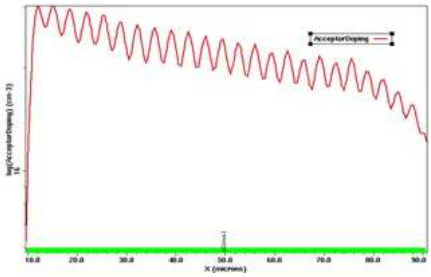

Fig. 4

did. The characteristics of the simulated device and those of the silicon device were similar in nearly every detail.

3 Result and Discussion

Figure 4 shows the surface electric field distributions along the drift region for the three different design regions of the device. Figure 5 shows a 2D simulation for the flat region with linear P-top structure of its surface electric field distributions. When the polarities are reversed, the impact ionization generation rate creates a weak point in the vertical n/p junction boundary. The critical electric field can be reduced by including more n/p junctions in the N-drift surface. The linear P-top dose is large in comparison to the N-drift region charge. The maximum BV is determined by the surface electric field and distance. The surface electric field of the linear P-top is highly uniform throughout the entire N-drift region, leading to an excellent breakdown voltage. If the windows of the P-top mask are optimized, the device can achieve an almost flat electric field, with less than 2.5 10^5 V/cm for the maximum BV and good reliability for lower electric field peaks near the source side.

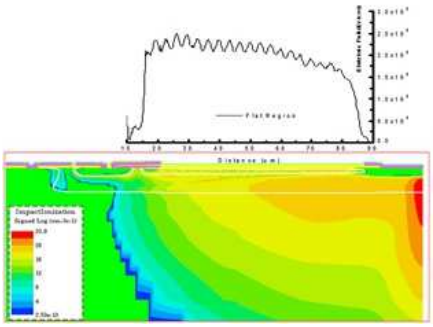

Fig. 5

The layout design of a race-track LDMOS structure was conceived. The actual product dies were labeled DC and SC. For the flat region, 2D processing and device

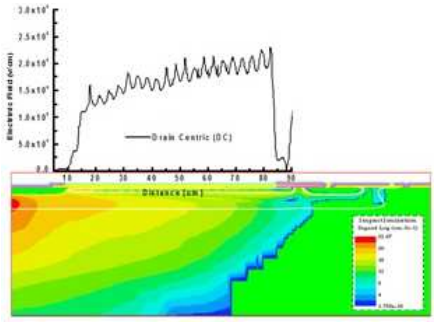

Fig. 6

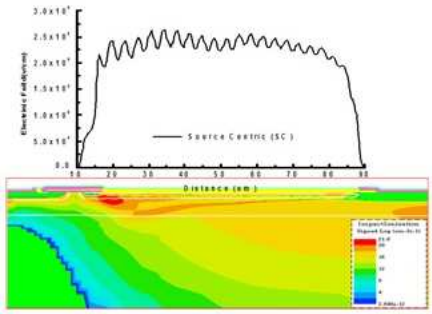

Fig. 7

simulations were performed to optimize the critical processes and geometrical parameters, and cylindrical layouts for DC and SC requirements were simulated. DC and SC have different and opposite behavior with respect to surface concentration versus breakdown degradation. The maximum breakdown voltage has been achieved at DC and SC regions of racetrack or cylindrical layout has been achieved through varying mask design while reducing surface electric field to address current crowding effect. Figure 6 shows a cylindrical simulation of a DC surface electric field with a maximum peak in the N-drift region and P-body. The simulated ideal SC surface electric field distribution and the impact ionization generation rate are shown in Fig. 7. The cylindrical layout effects and characteristics of the device were investigated. The 3D breakdown voltage was found to be lower than the 2D breakdown voltage, while the radius of curvature and the crowding effect showed much a higher leakage current, indicating a higher local electric field [12], [13]. Figure 8 shows the sensitivity window of the breakdown voltage as a function of P-top dose by 2D/3D TCAD simulation, for three linear mask designs, marked DC, SC and flat region. The plateau of the breakdown voltage curve provides the best window for manufacturing tolerances. Three regions near the linear P-top are simultaneously formed using the same implanting process so that different linear masks can adjust the charge balance with the surface electric field. To optimize the

device, one must maximize BV, minimize current crowding in the DC and SC regions, and minimize Ron.sp; moreover, one must increase the drift region doping as much as possible. [7], [11] The mask design of the linear P-top is crucial in achieving a desirable BV and the lowest possible Ron.sp. An optimal linearly-graded drift region doping profile can lead to a uniform distribution for the surface electric field as well as a linearly-graded electrostatic potential, resulting in low Ron.sp and high BV.

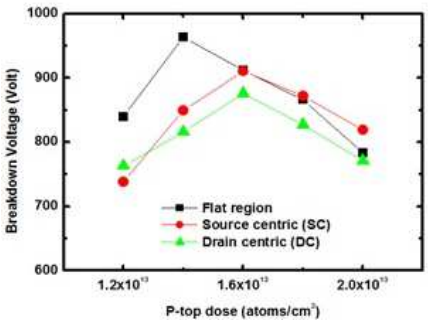

Fig. 8

The experimental results for the safe operation area (SOA) of IdVd curves with a linear P-top and a dual-channel conduction path in a UHV device with an off-state BV of about 842 V are presented in Fig. 9. Optimization of the N-top implant forms an extra conduction path over the P-top, which increases the conduction area and the current flow and thus reduces the Ron.sp. Figure 10 shows the experimental data for IdVg curves with and without an N-top layer implanted. The transistor has a threshold voltage of 3.2 V and a specific Ron.sp of 145 $m\omega - cm^2$. If the drain current improves by approximately 25%, the Ron.sp improves by approximately 25% because the N-top layer provides a dual-channel conduction path [9], [14]. Furthermore, the on-state of the device with an N-top yields a good IdVd curve, which is similar to the curve without an N-top, but presents a trade-off for the Ron.sp. Thus, we conclude that the device with an N-top layer has a lower Ron.sp.

The dependence of the surface potential and electric field distributions on linear P-top dose implantation for different P-top mask designs and the tuning of the charge balance have been comprehensively discussed. A method to produce optimally high voltage and good Ron.sp for the linear P-top LDMOS device has been proposed. Finally, the N-top layer for a dual-channel conduction path reduced Ron.sp by 25%, compared with the different existing technologies with linear P-top LDMOS performance, as shown in Fig. 11. A proposed N-top layer implantation can maintain the breakdown voltage at 842 V and reduce Ron.sp to 145 $m\Omega - cm^2$. [15], [16].

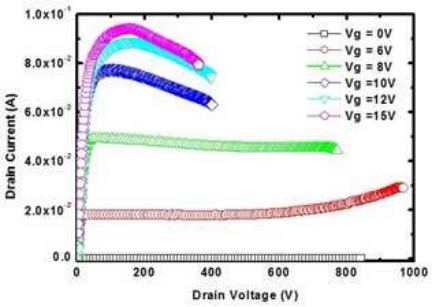

Fig. 9

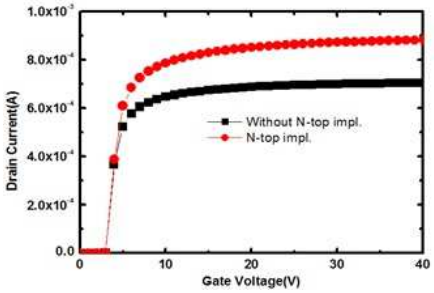

Fig. 10

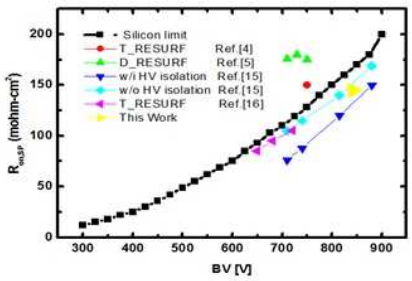

Fig. 11

4 Conclusion

We developed DC and SC design optimizations for an 800 V double RESURF LDMOS device with low Ron.sp and BV. An analytical model of a P-top mask based on a linearly-graded drift region shows excellent device improvement in the LDMOS device. TCAD simulations indicated that the P-top LDMOS exhibits BV of 800 V. By implanting an arsenic N-top layer over the P-top, one can improve Ron.sp by 25%. The device was successfully fabricated and the simulation results are in agreement with the silicon results.

Acknowledgement

The author would like to thank NUVOTON Technology Corporation. The authors would also like to thank National Center for High-performance computing, National Nano Device Laboratories and National Chip Implementation Center for providing the MEDICI and TSUPREM-4 software.

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