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FPGA Based Implementation of the Push-Pull Configuration of a Single Phase Multilevel Inverter with a Novel PWM Technique

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Abstract: This paper presents a new topology for a multilevel inverter, which consists of a single dc voltage source with a series of capacitors, power switches and a mid-point transformer to demonstrate the operation of a five level inverter. A SPARTAN 3E field programmable gate array based controller is used for the generation of the switching scheme. The comparative study of the proposed inverter with the classical one is also presented. The conduction and switching losses of the proposed topology are also calculated for the validation of the proposed topology. The performance of the proposed inverter is obtained using MATLAB simulation with R and R–L loads. The simulation results are validated by the experimental prototype results.

Keywords: Multilevel Inverter (MLI), Push-Pull, Field Programmable Gate Array (FPGA), Pulse width modulation (PWM)

1 Introduction

Inverters are power electronic circuits which convert dc to ac power. They can be classified as voltage source inverters (VSI), and current source inverters (CSI). The inverters can generate only two levels in the output voltage. Hence, the output voltage contains more harmonics. The Pulse width modulated (PWM) strategy is used to reduce the low frequency harmonic components for the two level output voltage. Though PWM inverters reduce the harmonics for the output voltage, they have many disadvantages; hence power electronic researchers are moving towards multilevel inverters (MLI) [1]. They have many advantages such as low total harmonic distortion (THD), minimized switching and conduction losses, reduced dv/dt, low electromagnetic interference (EMI) problems and reduced voltage stress across the switches. Multilevel inverters (MLI) have gained popularity in the field of static reactive power compensation, flexible AC transmission systems (FACTS), and isolated and grid connected renewable energy systems [2].

The classical MLI structures are the cascaded H-bridge multilevel inverter (CHBMLI), flying capacitor multilevel inverter (FCMLI), and the diode clamped multilevel inverter (DCMLI). Each MLI uses a different technique to generate the ac output voltage. The major disadvantages of the DCMLI are, it requires excessive clamping diodes when the number of level increases and they cannot control the real power flow. The demerits of the FCMLI are, more number of bulky power capacitors are required to generate high level on the output side. Compared with the DCMLI and FCMLI, CHBMLI requires the least number of components to generate the same level of output voltage. But, CHBMLI uses many sources to generate the multilevel output voltage [3]. From this discussion, it is concluded that MLI required more number of power electronic devices and gate drivers. This creates circuit intricacy and control difficulty. Nowadays, to defeat the above problems, lots of topology has been presented [4–17].

This paper proposes a novel transformer based multilevel inverter, with reduced number of power electronic switches and gate driver circuits. The proposed topology has inherent merits like isolation between load and supply, and the conduction and switching loss are minimized.

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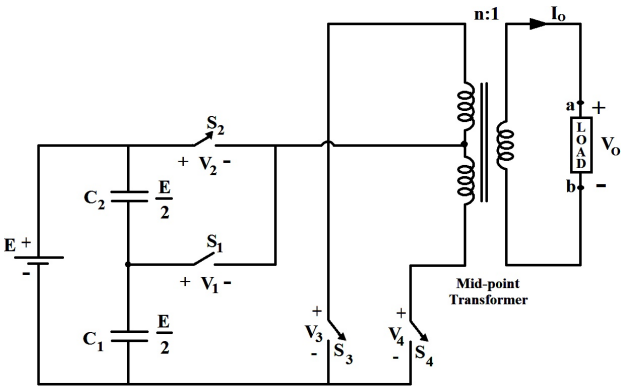


Fig. 1: Circuit diagram of the proposed push-pull multilevel inverter topology.

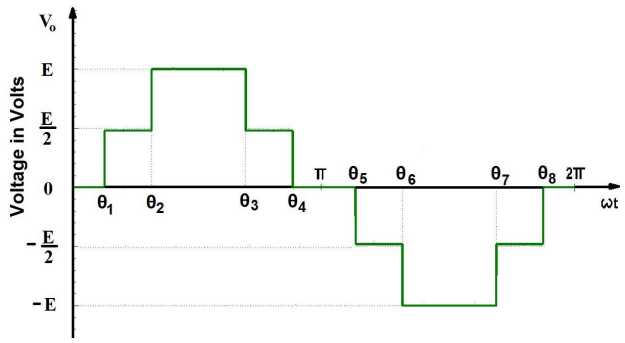


Fig. 2: Five level inverter stepped output voltage.

2 Proposed Inverter Topology

The proposed push-pull configuration of the single-phase five-level inverter consists of 3 unidirectional power switches, one bidirectional switch, and two equal value capacitors called as a voltage divider network, as shown in Fig. 1. The voltage divider network is used to divide the supply voltage. Each equal value capacitor has a voltage of $E/2$. Hence, the proposed topology can produce five levels of output voltage such as E, $E/2$, 0, $-E/2$, $-E$. The load is connected to the inverter through a mid-point transformer.

To understand the mode of operation of the proposed five level inverter, a typical five level inverter output voltage is shown in Fig. 2. Here, the switching state of the proposed multilevel inverter is tabulated.

In switching Table 1, 1 indicates ON and 0, OFF. The operation of the proposed inverter is explained using five switching states as given in Table 1. Here, a red line is used for the current flow. The modes of the operation are explained below.

Table 1: Proposed multilevel inverter switching state.

Switching State				(V_o)
S_1	S_2	S_3	S_4	
0	1	1	0	$+E$
1	0	1	0	$+E/2$
0	0	0	1	0
1	0	0	1	$-E/2$
0	1	0	1	$-E$

2.1 Mode 1: Maximum Positive Output Voltage $(+E)$

In this mode of operation, switches S_2 and S_3 are in the ON condition. Hence, both capacitors C_1 and C_2 deliver energy to the load. The circuit current flows though switch S_1, one portion of the primary of the mid-point transformer and S_3 as shown in Fig. 3(a). The load is connected on the secondary side of the mid-point transformer. The circuit current flows in the a to b direction on the load side and the output voltage across the load is $+E$. If a load is an inductive one and the direction of the load current is the opposite, the current flows through body diodes D_{s2} and D_{s3}, and charges the capacitor network.

2.2 Mode 2: Half Positive Output Voltage $(+E/2)$

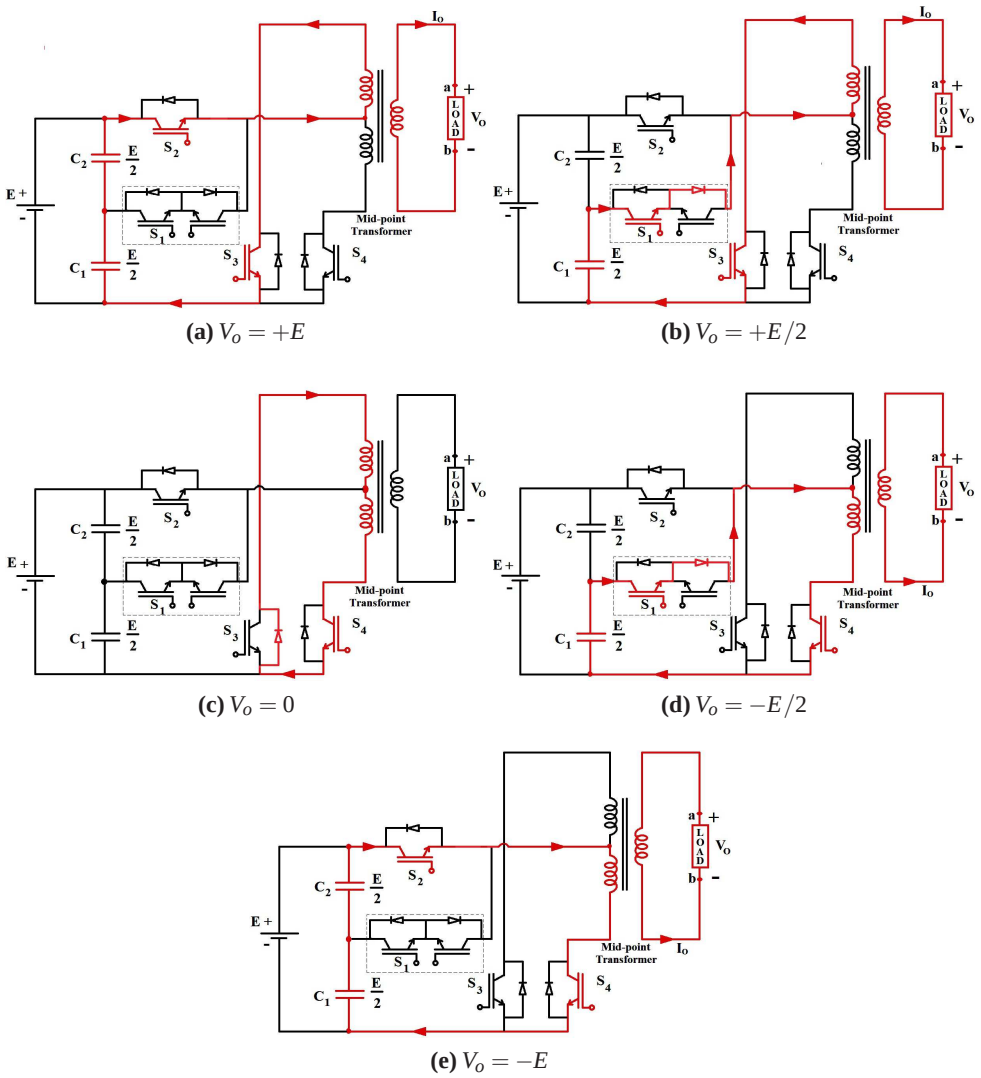
Here, the bidirectional switch S_1 and level modified switch S_3 are in the ON condition. The conduction path of the current flow is shown in Fig. 3(b). The capacitor C_1 delivers the energy to the load. The circuit current flows through the bidirectional switch S_1, one portion of the primary of the mid-point transformer and switch S_3. In the case of an inductive load, the current flows through the body diode of D_{s3} and the bidirectional switch S_1 charges the capacitor.

2.3 Mode 3: Zero Output (0)

In this mode of operation, the power electronic switch S_4 is in the ON condition and all other switches are in the OFF condition. Hence, short circuit happens in the primary winding of the mid-point and the voltage across the load is zero.

2.4 Mode 4: Half Negative Output Voltage $(-E/2)$

The bidirectional switch S_1 and unidirectional switch S_4 are kept in the ON condition to generate $-E/2$ voltage on the output side. The capacitor C_1 delivers energy to the load. The circuit current flows through the bidirectional switch S_1, another portion of the primary of the mid-point



(a) $V_o = +E$ **(b)** $V_o = +E/2$

(c) $V_o = 0$ **(d)** $V_o = -E/2$

(e) $V_o = -E$

Fig. 3: Modes of operation with current path.

transformer, as shown in Fig. 3(d). If the inductive load is connected on the load side, the current flows through the body diode D_{s4} and the bidirectional switch S_1 charges the capacitor.

2.5 Mode 5: Maximum Negative output $(-E)$

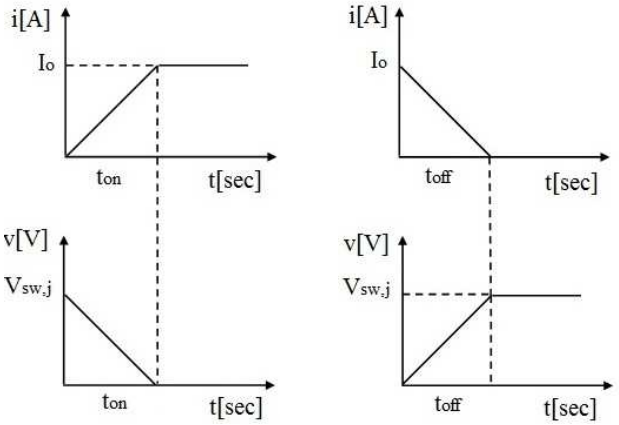
In this mode of operation, IGBT S_2 and S_4 are in the ON condition. The capacitor network (both capacitors C_1 and C_2) supplies the energy to the load. The circuit current flows through switch S_2, another portion of the primary of the mid-point transformer and the level modifying switch S_4. If the inductive load is considered, the current flows through the body diode D_{s4} and D_{s2} charges the capacitor network.

3 Power Loss Calculations

The total power loss is calculated by a summation of the switching loss and conduction loss. The power loss calculations in detail are as follows.

3.1 Switching Loss

The switching losses are calculated for a typical switch, and then these results are extended to the proposed multilevel inverter. The switching waveforms are represented by a linear approximation to the actual waveforms in order to simplify the discussion, as shown in Fig. 4 During the turn on and turn off interval, large values of switch voltage and current are present simultaneously [18].



(a) During turning on. **(b)** During turning off.

Fig. 4: Current and voltage waveforms of a switch.

The Energy dissipated in the device during the turn on period can be expressed as follows:

$$W_{on,j} = \int_0^{t_{on}} v(t)i(t)dt. \tag{1}$$

$$W_{on,j} = \int_0^{t_{on}} \left[\left\{ V_{sw,j} \frac{t}{t_{on}} \right\} \left\{ -\frac{I_o}{t_{on}}(t - t_{on}) \right\} \right] dt \tag{2}$$

$$W_{on,j} = \frac{1}{6} V_{sw,j} I_o t_{on} \tag{3}$$

The energy dissipated in the switch during the turn off period can be written as

$$W_{off,j} = \int_0^{t_{off}} v(t)i(t)dt \tag{4}$$

$$W_{off,j} = \int_0^{t_{off}} \left[\left\{ V_{sw,j} \frac{t}{t_{off}} \right\} \left\{ -\frac{I_o}{t_{off}} (t - t_{off}) \right\} \right] dt \tag{5}$$

$$W_{off,j} = \frac{1}{6} V_{sw,j} I_o t_{off} \tag{6}$$

The total switching loss (P_s) can be calculated as,

$$p_s = \sum_{j=1}^{N_C+2} \left[\frac{1}{6} V_{sw,j} I_o \left(t_{on} + t_{off} \right) f_j \right] \tag{7}$$

where f_j is the switching frequency, and the jth switch makes f_j number of transitions. In classical topologies all the switches are operated at a high switching frequency (f_s), but in the proposed topology ($N_{IGBT} - 2$) switches are operated at high switching frequency, and the remaining two switches are operated in the fundamental frequency (f_o). Hence, the switching power loss equation for the proposed topology can be expressed as

$$p_s = \delta \left\{ \sum_{j=1}^{N_c} \left(\frac{j}{2} \right) E f_s + 2(2E) f_o \right\} \tag{8}$$

where $\delta = \frac{1}{6} I_o (t_{on} + t_{off})$ is constant.

From Eq. (8), it is understood that the proposed topology has incurred less switching power loss compared to other topologies.

3.2 Conduction Loss

The instantaneous conduction loss of a typical insulated gate bipolar transistor (IGBT) is:

$$p_c T(t) = [V_T + R_T i^{\alpha}(t)] i(t) \tag{9}$$

The instantaneous conduction loss of a typical diode is

$$p_c D(t) = [V_D + R_D i(t)] i(t) \tag{10}$$

where V_T, and V_D are the on state voltage drop of the IGBT and the diode. R_T, and R_D are equivalent to an on-state resistance of the IGBT and the diode, and α is the gain constant of IGBT. The average conduction loss can be expressed as,

$$p_{c_{(avg)}} = \frac{1}{\pi} \int_0^{\pi} \Big[\{N_T(t) V_T + N_D(t) V_D\} i_o(t) + \{N_T(t) R_T i_o^{\alpha+1}(t)\} + \{N_D(t) R_D i_o^2(t)\} d(\omega t) \Big] \tag{11}$$

where $N_D(t)$ and $N_T(t)$ are the numbers of conducting diodes and transistor devices, respectively. In the proposed topology, only two switches bear 2E and the voltage across the remaining switches is (j/2) E. The conduction loss for the proposed multilevel inverter can be calculated from the following equation:

$$p_{c(avg)} = \sum_{j=1}^{N_C} \left(\frac{j}{2} \right) E I_o + I_o^2 R_T + 2(2E) I_o + \sum_{j=1}^{N_c - 1} V_D I_o + I_o^2 R_D \tag{12}$$

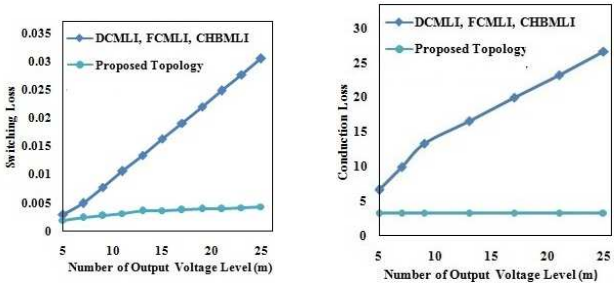
In the proposed inverter, the level modulated switches have a PIV of less than or equal to E, and the remaining two polarity changed power switches have a PIV of 2E. The total loss in the power switch is,

$$p_{losses} = p_{c(avg)} + p_s \tag{13}$$

Fig. 5(a) shows that the switching power loss of the proposed topology is lower than that of the conventional topologies. Fig.5(b) shows that the proposed topology has lower conduction loss than the other topologies.

4 Investigation of the Simulation and Experimental Results

A MATLAB simulation is carried out to validate the performance of the MLI. The proposed push-pull five



(a) Switching Loss. **(b)** Conduction Loss.

Fig. 5: Comparison of the losses of the proposed topology and other classical topologies.

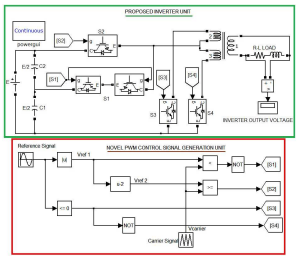


Fig. 6: Simulink model of the proposed push-pull five level inverter with the novel PWM control signal generation unit.

level inverter simulink model is shown in Fig. 6. This model provides IGBTs, capacitors, mid-point transformer and an R–L load. The comparison between the single triangular signal and two unidirectional offset sinusoidal signals provides the generation of the switching signal. In this study, the proposed inverter uses an input voltage of 40 V dc source. Each capacitor has a value of 330 μF with an equal voltage of 40/2 V. Here, the R load with the value of 85 Ω and the parameters of 40 Ω and 60 mH for the R–L load are assumed for the simulation and experimental investigation. The experimental prototype model photograph is in Fig. 7.

The Hardware model uses IGBT (H15R1203) along with the internal anti parallel diode. FPGA (Xilinx Spartan-3E XC3S100E) helps in the implementation of the PWM controller scheme. The generated gating signal is given to the gate driver circuit (IC-TLP250) and then fed to the IGBTs.

The experimental gating signal for the proposed multilevel inverter is shown in Fig. 8. The polarity changed switches S_3 and S_4 are operated at a fundamental frequency.

The output voltage and current waveform are simulated for the R and R–L loads and the results are shown in Figs. 9 and 11. The experimental output voltage and current waveform for the R and R–L loads are shown in Figs. 10 and 12. The Simulation results are match with the hardware load voltage and current waveforms. Hence,

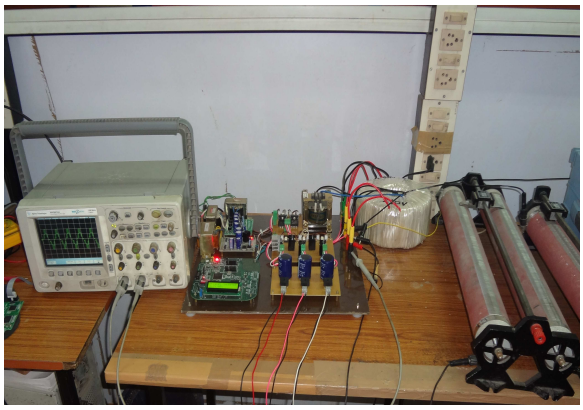


Fig. 7: Photograph of the Experimental set-up.

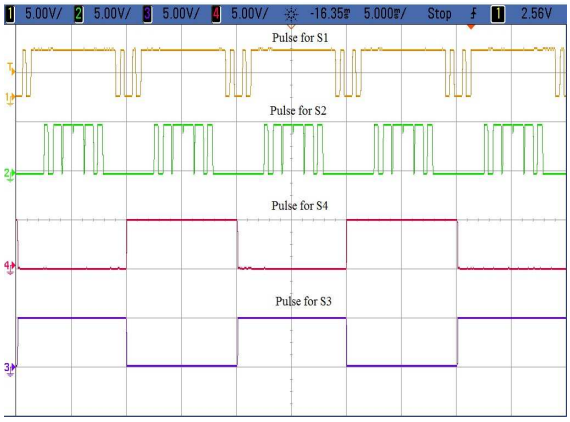


Fig. 8: Experimental Pulse pattern.

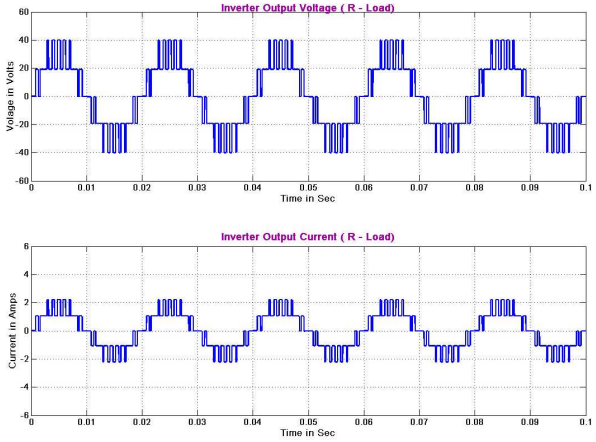


Fig. 9: Simulated Output Voltage and Output Current Waveform (R load).

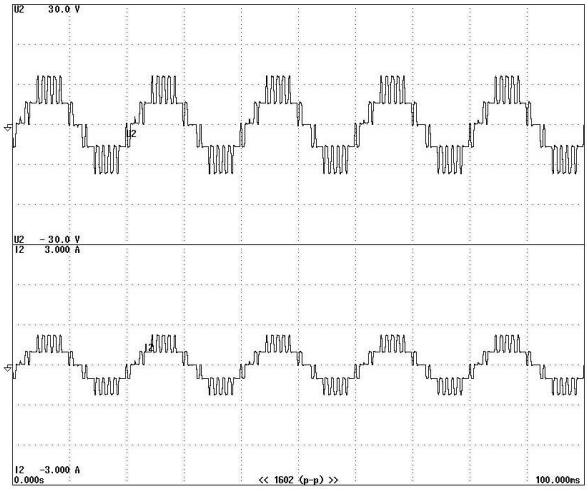


Fig. 10: Experimental Output Voltage and Output Current waveform (R load)

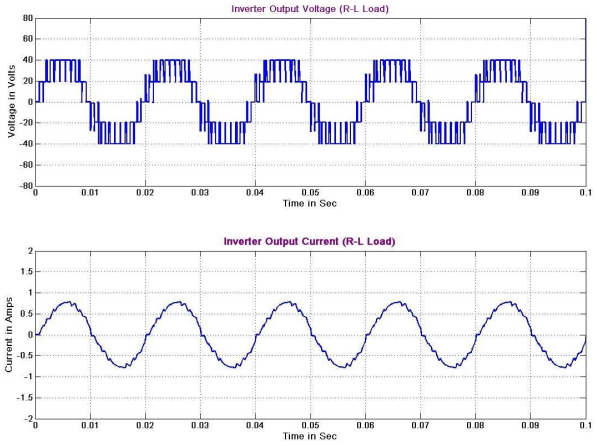


Fig. 11: Simulated Output Voltage and Output Current (R–L load).

the proposed topology is the best replacement for the inverter circuit and recommended for renewable energy applications. The Simulation results and the theoretical analysis of the proposed multilevel inverter are validated by the experimental results.

The simulated and the experimental current and voltage harmonic spectra of the proposed push-pull five level inverter with the R–L load are shown in Figs. 13, 14 and 15 respectively. The simulation and experimental results give the total harmonic distortion (THD) in the inverter output voltage of 21.28% and 22.17% respectively, for the R–L load. But the presented topology in [9] has a voltage THD value of 36.89%. The proposed topology output voltage has less total harmonic distortion compared with the other topologies.

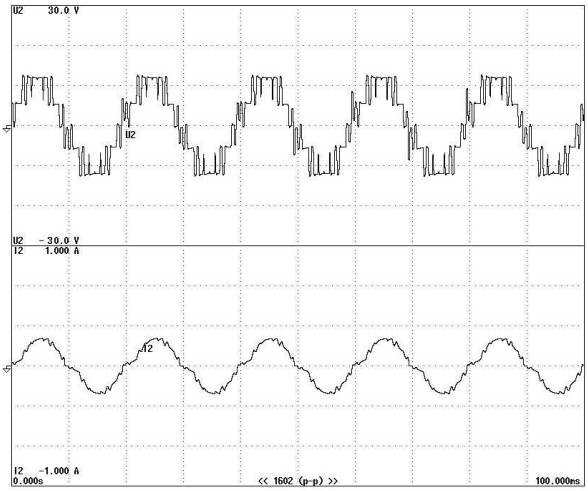


Fig. 12: Experimental Output Voltage and Output Current (R–L load).

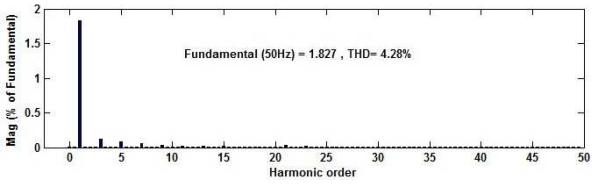


Fig. 13: MATLAB Output Current harmonic spectrum of the proposed push-pull five Inverter with R–L Load (without filter).

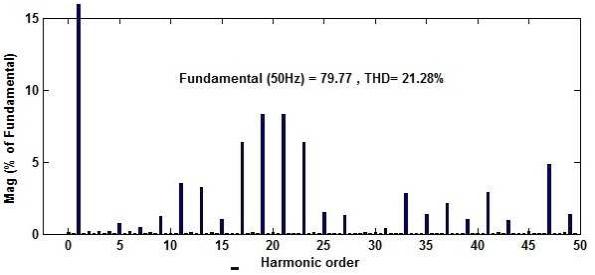


Fig. 14: Simulated voltage harmonic spectrum of the proposed push-pull five Inverter with R–L Load (without filter).

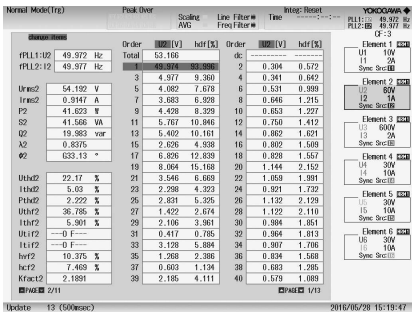
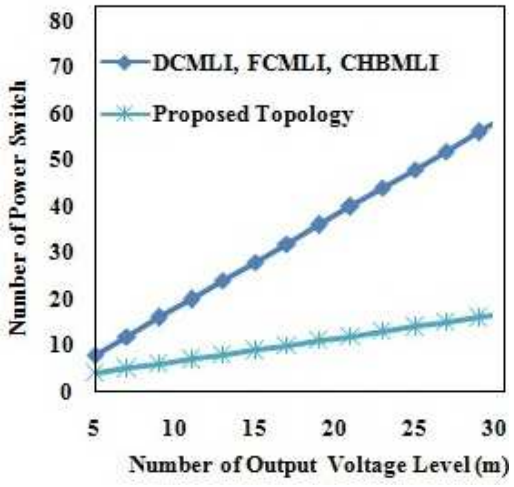


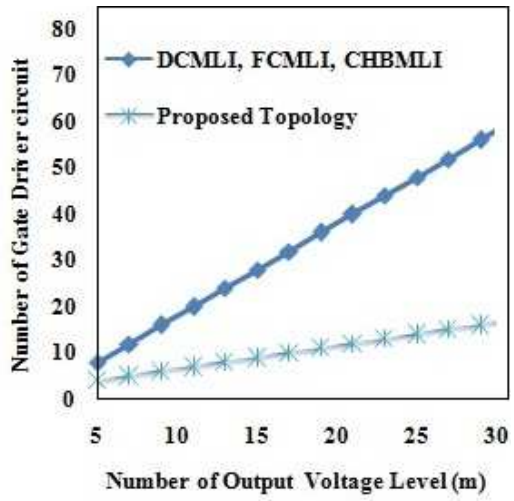
Fig. 15: Power quality analyser harmonic content for R–L load.

Table 2: Assessment of the power components requirement for 5 level inverter.

No. of Components	DCMLI	FCMLI	CHBMLI	Proposed Topology
Power Switches	8	8	8	5
Main Diodes	8	8	8	5
Clamping Diodes	6	0	0	0
Flying Capacitors	0	3	0	0
DC link capacitors	4	4	0	2
Input DC sources	1	1	2	1
Gate driver circuits	8	8	8	4
Transformers	0	0	0	1
Total components	35	32	26	18



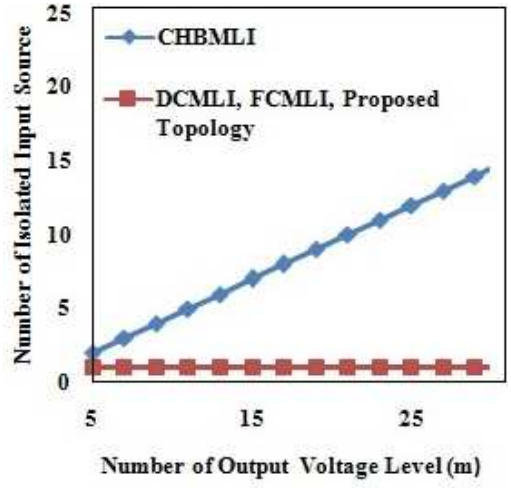
(a) Power Switches with respect to number of levels.



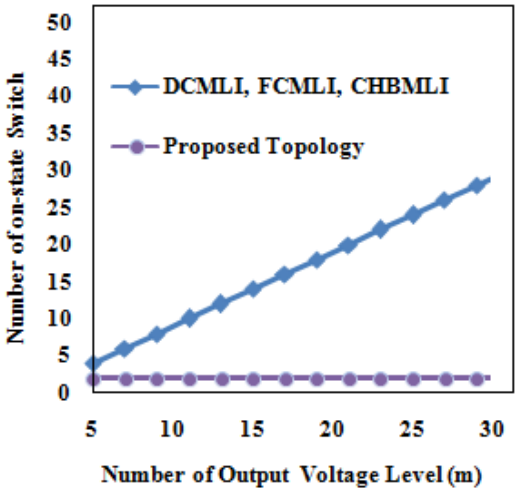
(b) Gate Drives with respect to number of levels.

5 Comparative Study

The main purpose of this work is the reduction of switches in a multilevel inverter, because increasing the number of power switches leads to an increase in the



(c) Sources with respect to number of levels



(d) On-state switches with respect to number of levels.

Fig. 16: Comparison charts.

inverter circuit size, cost, and control complexity. Compared to all the existing multilevel inverters, the proposed topology requires fewer numbers of components. Table 2 presents the number of components required to implement the five level inverter, using the proposed topology and three classical topologies. Fig. 16(a) show that the recommended topology needs fewer numbers of switches for generating an m-level output voltage. In this work, the five level inverter is implemented using only five switches. The proposed topology could achieve a 37.5% reduction in the number of power switches required, compared with the three classical topologies. The gate driver consists of the isolator and driver circuits. The isolation could be provided using either the pulse transformer or the opto-coupler. Fig. 16(b) presents the comparison of the gate drivers required for the proposed topology with other existing structures. The proposed topology utilized only 50% of the gate driver compared with the three classical

topologies. The gate drive reduction leads to reduce complexity in the circuit and minimize the cost.

Fig. 16(c) shows the comparison between the proposed topology and the existing topologies, in terms of the number of isolated input dc sources with respect to the number of output voltage levels. The proposed topology requires only one isolated dc source, whereas CHBMLI requires more number of isolated dc sources. Another major factor is the on-state switches that are important for the operation of the multilevel inverter. Fig. 16(d) shows the assessment of the numbers of on-state switches with the proposed topology, and the three classical topologies. In the proposed topology, two power switches are in the ON condition to provide any level of output voltage and loss of conduction is reduced. It is understood that to increase high voltage output from a low voltage source, additional components or step-up transformers are required in the classical multilevel inverters. From this comparison, it is concluded that the proposed topology could achieve a 49%, 44% and 31%, reduction in the total number of components required to implement the inverter structure compared with DCMLI, FCMLI and CHBMLI respectively.

6 Conclusion

In this paper, a new single phase push-pull multilevel inverter has been developed. A novel PWM switching scheme for the proposed topology has been implemented in the FPGA controller. The Comparison analysis shows that a minimum number of switching devices, gate drive circuit and on state switches are used in the proposed multilevel inverter. Also, due to the reduction of switching and conduction losses the efficiency of the proposed MLI is increased. The performance of the proposed inverter is obtained using MATLAB simulation with R and R–L loads. The simulation results are validated by the experimental prototype results.

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