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Design and Mathematical Evaluation of a New Multilevel Inverter Topology with Less Circuit Components for Solar and Wind Energy Conversion Systems

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Abstract: Multi level inverters are capable of synthesizing a near sinusoidal voltage at its terminals from multiple dc sources. The quality of synthesized output waveform depends on the parameters like number of voltage sources/capacitors, components employed in the inverter and modulation technique used to control the inverter. In this paper a multilevel inverter topology with reduced switch count has been designed. It can be used for interfacing wind and solar energy conversion systems to conventional grid. The topology has been mathematically evaluated against the similar topologies in the literature in the aspects of number of IGBTS required, driver circuits required and diodes required. The terminal voltage and the voltage THD of the inverter has been tested with two modulation schemes, they are Sinusoidal-Multicarrier Pulse Width Modulation (S-MPWM) and Nearest level Modulation Scheme (NLM). The observation concluded that even though the output THD of the inverter is high When NLM is used, the switching losses are greatly reduced. The simulations are carried out using MATLAB SIMULINK software package and the results are verified with a NLM controlled prototype.

Keywords: Multilevel inverter, Cascade H-Bridge, Nearest Level Modulation, Symmetric Multilevel Inverter.

1 Introduction

In the conventional voltage source inverters the terminal voltage resembles a square wave; a multilevel inverter is capable of delivering a near sinusoidal stepped terminal voltage. The number of steps in voltage waveform is influenced by the number of independent voltage sources/capacitors deployed in the input [1]. This makes the multilevel inverter more suitable for solar PV applications. As the solid state technologies for high voltage applications are still a grey area, multilevel inverters can be deployed in high voltage applications with matured low and medium voltage switches. The traditional multilevel inverter topologies are classified as Neutral Point Clamped (NPCMLI) [2], Flying Capacitor (FCMLI) [3] and Cascaded H-Bridge [4].

A neutral point clamped inverter comprises of capacitors connected in series with a neutral point of a common dc bus and $n-1$ clamping diodes. The number of capacitors connected in series on either side of the neutral point of dc bus is dependent on the number of levels n required in the terminal voltage waveform [5]. However in NPC inverter topology, voltage unbalancing problem arises during transfer of real power [6]. In addition to that, NPC multilevel inverter requires huge volume of diodes if the desired number of steps in the terminal voltage is high. Flying Capacitor (FCMLI) topology which is otherwise called as Capacitor Clamped Multi-Level Inverter (CCMLI) is similar to NPC multilevel. Unlike the diodes, the voltage cannot be blocked or reversed through the capacitors; therefore in FCMLI a given voltage level can be obtained through multiple switching combinations. This makes it highly redundant when compared to NPCMLI. However the component count in CCMLI is as high as NPCMLI [7] and the circuit becomes bulky with larger capacitor banks for higher voltage levels [8]. Cascaded H-Bridge inverters can be derived by cascading multiple H-bridges. The cascading effect aid in obtaining medium or high terminal voltage levels with low voltage switches matured in technology [9]. The CHB inverters are highly modular in nature and can be extended when need arises. But, the required number of switches and number of independent voltage sources will increase rapidly when the desired steps in terminal voltage is high.

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The recent research is focused on reducing the cost and improving the reliability of the CHB converter topology by reducing the number of switches and number of gate driver circuits for the given number of levels. A new structure for the multilevel inverter with a reduced number of power electronic components is described in [10]. Apart from the switches in the H bridge the other switches in the module are bidirectional switches. Therefore for n number of sources the proposed structure requires 2*n*+4 switches and *n*+4 gate driver circuits. This number will increase rapidly if the number of modules of the converter is increased. The switch count and the number of gate driver circuits have been brought down to 2*n*+2 and *n*+4 respectively in [11].

In the topology proposed in [12], only odd number of sources is considered. In order to increase the number of levels, a module containing two sources have to be added for every rise and the number of switches increases by 4 for the addition of every such module. This makes the circuit bulky for higher number of levels. In [13] a new topology called semi cascaded inverter has been introduced. The number of switches and the peak inverse voltage of the inverter are reduced when compared to [12]. But, there is a possibility of voltage sources getting short circuited due to commutation delay. A new semi cascaded inverter has been presented in reference [14] but this can be employed only as a symmetric configuration.

A new topology has been suggested in [15]. In this topology two sources and two capacitors have been used for a nine level inverter. The number of levels can be extended up to desired value. In the nine-level inverter described in [15], there is a module with one controlled switch and four diodes connected between capacitors. If we consider the number of capacitors as N_c, then there will be $N_c - 1$ number of such modules will be present in the circuit. This drastically increases the number of diodes utilized in the converter circuit. This makes the circuit bulky and the reliability of the converter will be reduced. An advanced configuration for symmetric multilevel voltage converter has been presented in [16]. The author implemented a symmetric multilevel inverter in two configurations viz., with odd number of sources and with even number of sources. A group of sub-cells were a sub-cell comprising of two sources and four switches are used for even number of sources. An additional source has been used with the above said sub cells for odd number of sources. The number of switches increases when the number of sources is high.

This paper proposes a Z-Armed Multilevel Inverter with reduced switch count. The proposed multilevel inverter can be employed in both symmetrical and asymmetrical configurations. The successive content of the paper is organized as follows 1. Construction of proposed topology 2. Establishing mathematical relations for required components, 3. Comparative analysis with other similar topologies in the literature, 4. Simulation studies 5. Evaluation of losses, 6. Experimental verification.

2 Proposed Topology

The basic unit of the proposed Z- Armed Multilevel Inverter is shown in Fig.1 This topology comprises of an H - bridge for polarity reversal and a level adder with independent DC sources for synthesizing required levels in the terminal voltage waveform. The unidirectional switches without anti-parallel diodes are connected in series with independent DC sources in the shape of alphabet 'Z' as shown in the Fig. and so the topology can be called as Z Armed Multilevel Inverter (ZAMLI). The topology can be used in symmetric as well as asymmetric mode.

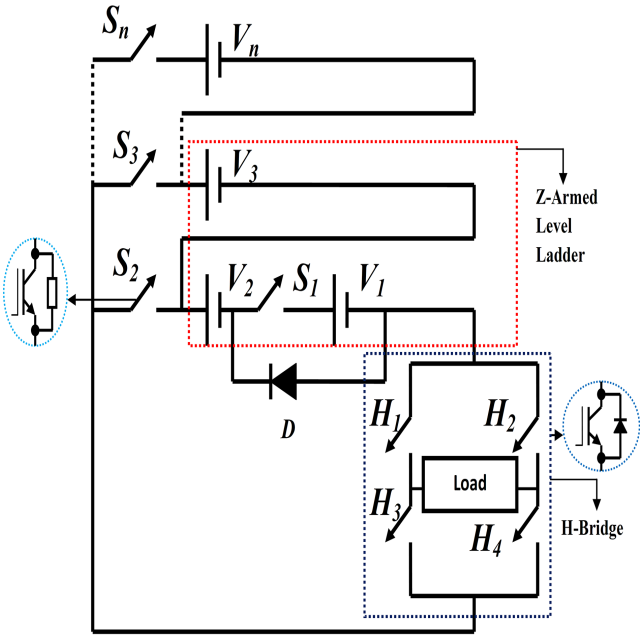


Fig. 1: Schematic of the proposed topology

2.1 Symmetric Configuration

In symmetric mode the terminal voltage of all the independent dc sources are equal. For the given *n* number of independent voltage sources, the number of level generated will be $2n + 1$. The number of switches required for symmetric configuration can be represented as in Eq (1).

$$N_{switch} = n + 4 \tag{1}$$

Excluding the diode, the number of controlled switches employed in the circuit can be represented using Eqn (2).

$$N_{IGBT} = n + 4 \tag{2}$$

The number of drivers required for the proposed ZASMLI can be given as in Eq (3)

$$N_{driver} = n+4 \tag{3}$$

Summarizing the Eqs (1),(2) and (3)

$$N_{switch} = N_{IGBT} = N_{driver} \tag{4}$$

The maximum output voltage across the H Bridge for a symmetric topology will be nV_{dc}, were V_{dc} is the voltage magnitude available from a single isolated voltage source and the voltage blocked across switches in level ladder, H-Bridge and the whole module can be represented as follows

The voltage blocked across the switches in level adder can be given as

$$V_{st} = V_{dc} \text{ for } i = 1,2,3,\ldots,n \tag{5}$$

The voltage across the switches in H-Bridge when turned OFF is

$$V_{HI} = nV_{dc} \tag{6}$$

The maximum blocking voltage across the inverter can be expressed as

$$V_{max} = (4n+n+1)V_{dc} \tag{7}$$

The magnitude of voltage obtained at the terminals of the level ladder for different switching combinations is depicted in table 1. In the table the value 1 implies that the concerned switch is in ON state and the value 0 implies the off state of the corresponding switch.

Table 1: Different possible switching states and the corresponding terminal voltage at level ladder

State	Switching States										Voltage
	S_1	S_2	S_3	S_4	$\cdots$	S_N	H_1	H_2	H_3	H_4	V_T
0	0	0	0	0	$\cdots$	0	1	1	0	0	0
1	0	1	0	0	$\cdots$	0	1	0	0	1	Vdc
2	1	1	0	0	$\cdots$	0	1	0	0	1	$2Vdc$
3	1	0	1	0	$\cdots$	0	1	0	0	1	$3Vdc$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
n	1	0	0	0	0	1	1	0	0	1	$nVdc$
$n+1$	0	1	0	0	0	0	0	1	1	0	$-Vdc$
$n+2$	1	1	0	0	0	0	0	1	1	0	$-2Vdc$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$2n$	1	0	0	0	0	1	0	1	1	0	$-nVdc$

2.2 Asymetric Configuration

The proposed topology can also be used in asymmetric configuration. In asymmetric mode of operation, the magnitude of voltage delivered by the independent sources connected in the basic structure will not be same. If only basic structure is used

$$V_1 \neq V_2 \neq \ldots \neq V_n \tag{8}$$

If cascaded

$$V_{11} = V_{12} = \ldots = V_{1n} \neq V_{21} = V_{22} = \ldots = V_{2n} \tag{9}$$

The magnitude of independent voltage sources can be chosen with an objective to maximize the number of levels and to minimize the number of switches. The standing voltage and the number of levels generated for different values of magnitude chosen can be obtained using the equations shown in table 2. From the table it can be understood that the maximum standing voltage, number of levels and terminal voltage depend on number of sources used and the magnitude of each source. If the number of sources and the magnitude of voltage are fixed then the topology can be simulated with the same control scheme developed for a symmetric mode and a similar stepped waveform can be obtained.

Table 2: Magnitude selection algorithm for asymmetric topology

Method	**Voltage magnitude of independent DC voltage sources, Volt**	**Standing Voltage, Volt**	N_{va}	N_{level}
Method 1	$V_{1i} = V_{dc}$, for $i = 1,2,3,\cdots,n$ $V_{2i} = 2V_{dc}$, for $i = 1,2,3,\cdots,n$ $V_{ki} = kV_{dc}$, for $i = 1,2,3,\cdots,n$	$5n + 1 \times (n(n-1)/2)V_{dc}$	k	$2\sum_{j=1}^{k}(n\times j)+1$
Method 2	$V_{1i} = V_{dc}$, for $i = 1,2,3,\cdots,n$ $V_{2i} = V_{11} + 2\sum_{i=1}^{n} V_{1i}$, for $i = 1,2,3....n$ $V_{3i} = V_{11} + 2\sum_{i=1}^{n} V_{1i} + 2\sum_{i=1}^{n} V_{2i}$, for $i = 1,2,3....n$ $V_{ki} = \prod_{i=1}^{k-1}(2n_i+1)V_{dc}$, for $i = 1,2,3....n$	$= (5n+1) + (5n+1)(2n+1) + (5n+1)(2n+1)^2 + \ldots\ldots + (5n+1)(2n+1)^{k-1}$	k	$\prod_{1}^{k}(2n_i+1)V_{dc}$

3 PWM Scheme

There are number of PWM schemes in the literature for controlling multilevel inverters. In this paper two PWM schemes called Multi Carrier PWM scheme (MCPWM) and Nearest Level PWM scheme(NLPWM) are considered. The control of proposed inverter has been simulated with both the control schemes and a suitable scheme for hardware fabrication is identified.

3.1 Sinusoidal-Multi-Carrier pulse width modulation

In sinusoidal carrier pulse width modulation the reference wave is compared with a triangular carrier wave to

generate the gating pulses. The frequency of the reference wave will be equal to the required output frequency. In the control of multilevel inverter multiple carrier waves are used as shown in Fig.2 There are several sinusoidal multiple carrier PWM techniques available in literature based on the type of carriers and modulating signals used. The train of pulses required to trigger the switches in the inverter is generated by comparing the reference wave with multiple carriers. If a carrier signal with magnitude (Peak to Peak) $A_{carrier}$ and a modulating signal with amplitude A_{ref} is considered, the modulation index can be expressed as

$$m_a = \frac{A_{ref}}{nA_{carrier}} \tag{10}$$

If the frequency of the carrier wave and the reference wave are considered as $F_{carrier}$ and F_{ref} respectively, the frequency modulation index can be expressed as in eqn.(11) [17].

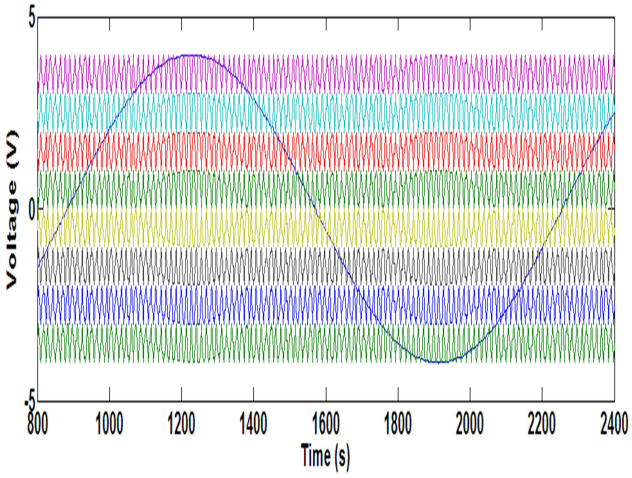


Fig. 2: Reference and Carrier waves

$$m_f = \frac{f_c}{f_{ref}} \tag{11}$$

3.2 Nearest level modulation scheme

The fundamental switching based nearest level control method is suitable for low switching frequency and high power applications. In this method, the switching signal for a given voltage step is generated by comparing the magnitude of desired voltage step with a constant rounded nearest to it as shown in the Fig.3. The control scheme for pulse generation is shown in Fig. 4. [18]

The magnitude of synthesized output step is given as shown in Eq (12), for example in level 1 the reference wave is compared with 0.5 and a resultant signal generated is used to produce gating signals for the concerned switches shown in table 1[18].

$$V_0 = V_{dc} round_{0.5}(V_{ref}) \tag{12}$$

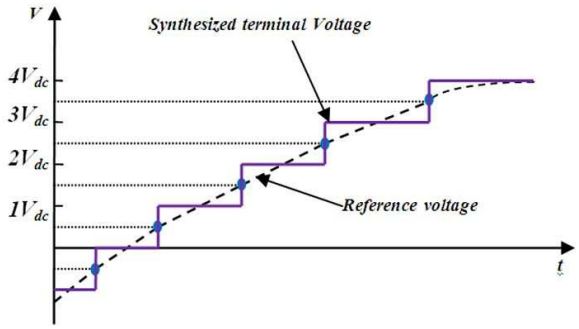


Fig. 3: Concept of Nearest level Modulation

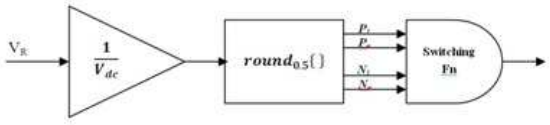


Fig. 4: Control scheme for pulse generation

4 Comparison of circuit components

The number of components required for the generation of desired levels in the terminal voltage of the inverter in symmetric configuration has been compared with different topologies as shown in table 3. As listed in table 3, the proposed topology has been compared with the topologies suggested in [11],[16] and [15] in the attributes like number of IGBTs, number of driver circuits and number of diodes required. The plots for the equations tabulated in table 3 are shown in the Fig.5. From the Fig.5a,5b and 5c, it can be understood that, for the given number of output voltage levels; the proposed topology requires less number of IGBTs, less number of driver circuits and less number of diodes respectively when compared to the topologies presented in the references [11] and [16].

From the table 3 one may come to a conclusion that the number of switches required for the topology

Table 3: Comparison of component required

Topology	**Number of controlled switches**	**Number of Gate drivers**	**Number of diodes**
Ref [11]	$2(n-1)+4$	$(n-1)+4$	$2(n-1)+4$
Ref [16] Proposed (a)	$4n+10/3$	$4n+10/3$	$4n+10/3$
Ref [16] Proposed (b)	$4n+14/3$	$4n+14/3$	$4n+14/3$
Ref [15]] (Nine levels-with two independent sources)	7	7	10
	If a capacitor is added to increase the level, then the number of switch will increase by 1 and the number of diodes increases by 4		
Proposed topology	n+4	n+4	5

suggested in [15] is less. But, when the number of sources or the required number of levels in the output increases, the number of required diodes will increase rapidly as shown in Fig.5 and this will affect the reliability of the topology.

5 Performance Evaluation

The performance of the proposed nine level topology is analyzed based on output THD, Converter losses and availability of redundant switching states. The inverter is simulated in MATLAB/SIMULINK environment. The parameters used for simulation are as follows $V_{dc} = 25V$, Snubber resistance of IGBT = $1e^5 ohms$, Internal resistance of IGBT= 0.001 *ohm*, Load resistance $R = 100 ohm$ and Load inductance = $50 mH$.

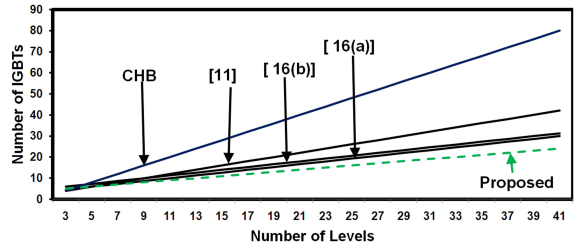
5.1 THD evaluation

Total Harmonic Distortion is the index used for computing the extent of harmonics in the given waveform it can be calculated as follows

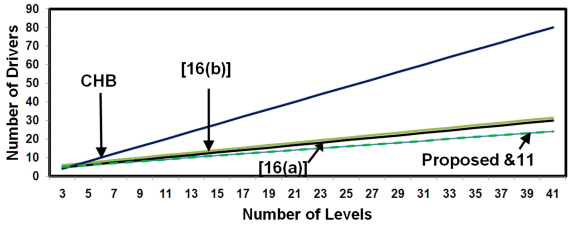
$$THD = \sqrt{\frac{\sum_{n=odd}^{\infty} V_{t.n}}{V_{t1}}} = \sqrt{\frac{V_{t,rms}}{V_{t1}} - 1} \qquad (13)$$

The simulated terminal voltage, current and harmonic spectrum of the proposed inverter with nearest level modulation scheme is shown in the Fig.6.

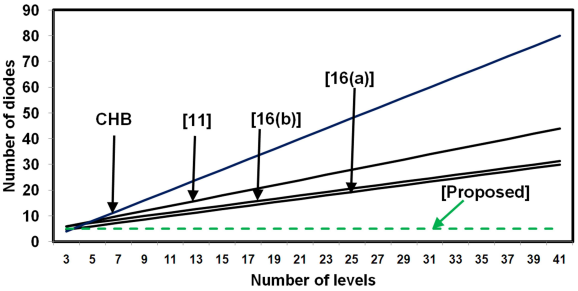
The proposed converter is also simulated with Sinusoidal-Multicarrier PWM technique shown in the Fig.2 The terminal voltage, load current and harmonic spectrum of the inverter simulated with Phase Opposition Disposition scheme is shown in the Fig.7



(a)Number of levels Vs IGBTs



(b)Number of levels Vs Drivers



(c)Number of levels Vs diodes

Fig. 5: Comparison of Number of levels Vs

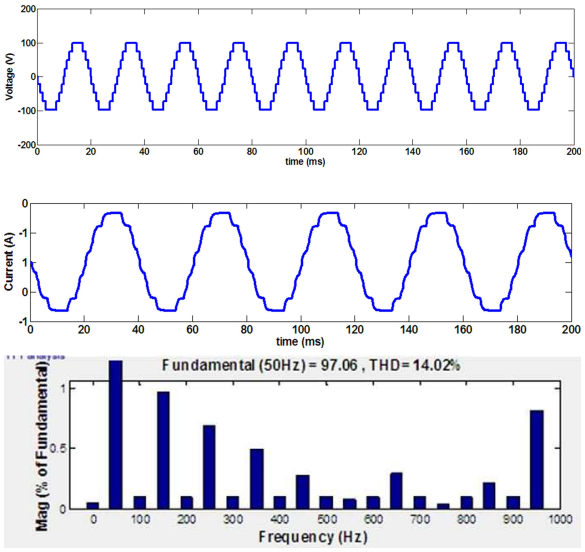


Fig. 6: (a) Load Voltage (b) Load current (c) THD

The number of independent dc sources used in both the cases is four. The magnitude of output voltage from each source is 25V. Thus for the given load resistance 100ohm and inductive reactance 20mH, the load current can be computed as 1A. The total harmonic distortion in the terminal voltage of the inverter is found as 14.02% as shown in Fig.6c. when the inverter is controlled using nearest level modulation scheme. The THD of the inverter while using sinusoidal multi carrier pulse width modulation is evaluated as 9.54% as displayed in the harmonic spectrum Fig.7. The voltage waveform is dynamic and thus the extent of nonlinearity is low when compared to its counterpart nearest level modulation. Therefore the THD of the terminal voltage will be low if sinusoidal multi carrier pulse width modulation scheme is employed.

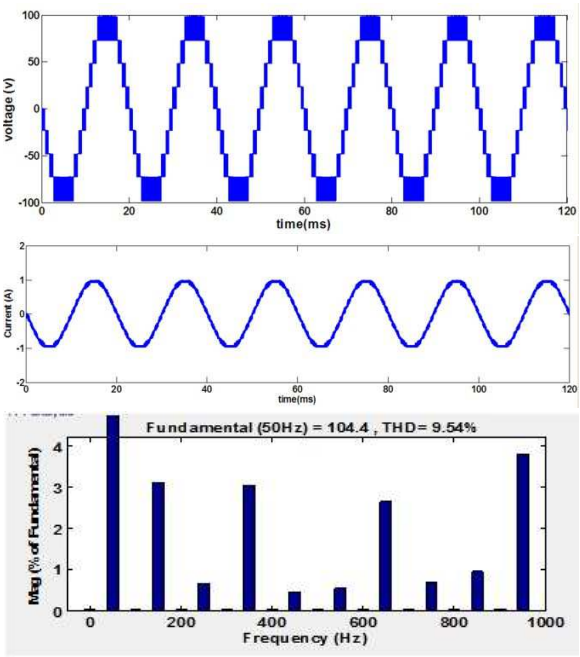


Fig. 7: (a) Load Voltage (b) Load current (c) THD

5.2 Evaluation of converter losses

The average switching and conduction power loss vary according to switching sequence and from the linearized model given in [19], The expression for average power loss across a switch can be written as below

$$= \frac{V_{BLOCK} I_C}{T_{total}} \left(\frac{T_{s-on} + T_{s-off}}{6} \right) + \frac{V_C I_C}{T_{total}} \left(T_{total} - T_{s-off} - T_{s-on} \right) \quad (14)$$

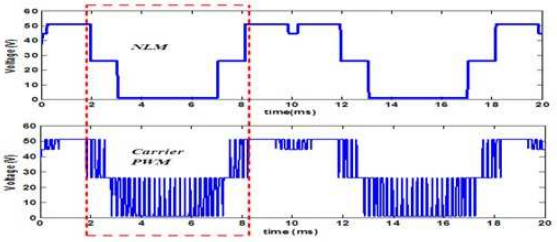


Fig. 8: Voltage blocked across the switch S3 in NLM method and S-MPWM

5.3 Switching Losses

In the Eq (14) the first component represents the switching loss per switching instant of a switch. [19]. For example during the time period 3 ms to 7 ms shown in Fig.8, if switch S3 controlled using Nearest Level Modulation scheme is considered, for a blocking voltage $V_{BLOCK} = 25V$, conduction current $I_c = 1A, T_{s-off} = 18\mu s, Ts-on = 10\mu s and T_{total} = 4ms$; The switching loss can be calculated as

$$P_{Switching} = \frac{V_{BLOCK} I_C}{T_{total}} \left(\frac{T_{s-on} + T_{s-off}}{6} \right) \quad (15)$$

$$P_{Switching} = \frac{50 \times 1}{4 \times 10^{-3}} \left(\frac{28 \times 10^{-6}}{6} \right) \quad (16)$$

The switching loss for the above switching instant calculated from Eq (16) is 0.058W. For the same values, if the Sinusoidal carrier PWM scheme is considered the number of switching instants in the given time period is high and hence the losses will be high

5.4 Conduction Losses

The loss that occurs due to the internal resistance of the switch is termed as conduction loss [19]. From the Fig.9 it can be understood that the voltage drop across the switch during the conduction period is 1V. The conduction current is 1A. In Eq (14) the second term represents the conduction loss per switching instant. With the above said values of Ts-on, Ts-off , Ttotal and a conduction current Ic the conduction loss across the switch can be calculated as

$$P_{Conduction} = \frac{V_C I_C}{T_{total}} \left(T_{total} - T_{s-off} - T_{s-on} \right) \quad (17)$$

$$P_{Conduction} = \frac{1 \times 1}{4 \times 10^{-3}} \left(\left(4 \times 10^{-3} \right) - \left(18 \times 10^{-6} \right) - \left(10 \times 10^{-6} \right) \right) \quad (18)$$

The conduction loss of the switch calculated from

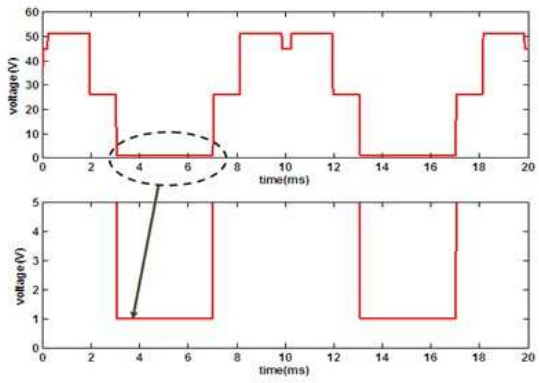


Fig. 9: Voltage blocked across the switch S3 in NLM method and Zoomed view during 3ms-7ms

equation (18) is 0.992 W. The total conduction loss of the inverter is proportional to number of switches in the topology. In that case the proposed topology which has lesser number of switches than the compared references will dissipate less power for the given power rating. The conduction losses depends on number of switches in the ON state for a given voltage level. As far as the proposed topology is concerned the number of switches turned ON during the generation of any voltage level is two.

6 Experimental results

The schematic of the prototype inverter is shown in the Fig.10 The nearest level modulation switching scheme has been embedded in a FPGA Spartan XE3S250E controller. The control circuits comprises of an opto-coupler, a schmitt trigger, and a buffer. The optocoupler provides isolation between the FPGA controller and the switches and the Schmitt trigger acts as an analog to digital converter. The experimental setup of

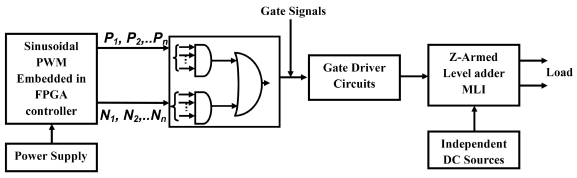


Fig. 10: Functional diagram of the fabricated prototype model

the prototype 9- level inverter is shown in the Fig.11. The load voltage and load current delivered by the prototype are as shown in Fig .12 The value of DC input voltage per

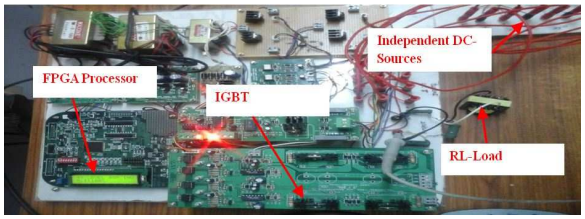


Fig. 11: Hardware Prototype

source chosen is 20V. Four independent DC voltage sources, 4 IGBTs with diode, 4 IGBTs without diode and 8 driver circuits are utilized. The technical specifications of the above said components are given in the table 4.

Table 4: Comparison of component required

S.No	**Description**	**Ratings**
1.	RL Load Values	R=100 Ohm and L=35mH
2.	IGBTs Model No: BUP400D	VCE=600V and IC=22A
3.	Gate Driver Circuits: HCPL316j	Drive Upto IC=150A and VCE=1200V
4.	Pulse Generator	FPGA Spartan XE3S250E
5.	V1=V2=V3=V4= 20 V	Vout=80V

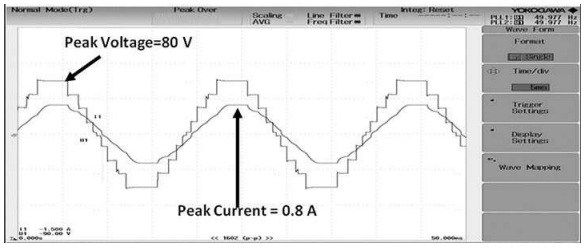


Fig. 12: Load Voltage and Load Current

From Fig.12 and Fig.13, it can be understood that the simulation results are close to experimental results and the proposed topology is capable of generating required number of steps in the terminal voltage waveform sequentially according to the control scheme used.

7 Conclusion

A Z-Armed Multilevel Inverter module is presented in this paper. The proposed module can accommodate *n* number independent voltage sources within itself and any number of such modules can be cascaded together. The circuit components required for this topology is less when

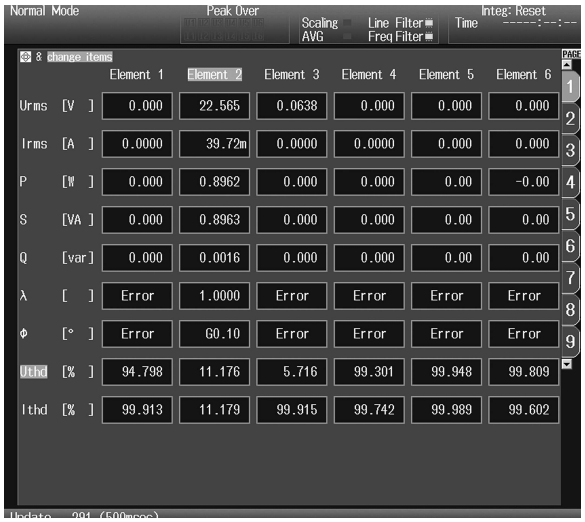


Fig. 13: Load Voltage THD

compared to other topologies presented in recent literature. Also, each voltage step other than Vdc i.e., $2V_dc$,$3V_dc$,... nV_dc can be obtained using two switching combinations. Therefore for n independent sources, the proposed topology can offer $2(n-1)$ redundant states. This makes the topology more redundant and reliable. The performance of the proposed topology is tested with two control schemes Nearest Level Modulation Scheme (NLM) and Sinusoidal carrier pulse width modulation (SPWM). The output THD of the inverter is low when controlled with Sinusoidal Pulse Width Modulation but the switching losses in the latter is high. The topology has been simulated in the MATLAB/Simulink environment and the simulation results are justified with a hardware prototype. Since, the number of components in the proposed circuit is very less the reliability of the circuit will be high with less conduction losses.

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