Applied Mathematics & Information Sciences
An International Journal

http://dx.doi.org/10.18576/amis/120617

Design and Performance Estimation of Efficient Approximate Carry Select Adder

V. S. Nishok[1,*], *P. Poongodi*[1] *and K. N. Vijeyakumar*[2]

[1] Department of Electronics and Communication Engineering, Kalaignar Karunanidhi Institute of Technology, Coimbatore, India
[2] Department of Electronics and Communication Engineering, Dr. Mahalingam College of Engineering and Technology, Coimbatore, India

Received: 2 Sep. 2018, Revised: 2 Oct. 2018, Accepted: 13 Oct. 2018
Published online: 1 Nov. 2018

Abstract: Carry select adder is the key circuit to achieve high-speed arithmetic operations. This paper presents the Efficient Approximation Carry Select Adder (EA-CSLA) involved in eradicating the carry 1 input path in LSB and attains a reduced amount of delay and hardware simplicity. Furthermore, this EA-CSLA utilizes an algorithmic cell split-up technique which diminishes the propagation delay in all parts of the circuit. The EA carry select adder design includes approximate full adder blocks with less gate count and reduced power consumption. This design is synthesized in Encounter-Cadence 90 nm tool up to GDSII level using Verilog language. Hardware implementation is done and verified through Xilinx System generator and the device Spartan 6 XSLX4T CSG324 is used. The EA carry select adder attains less area, reduced delay, error percentage and delay-entire power product than exact and present adders. The proposed efficient approximation circuit attains a considerable decrease in entire power utilization than existing approximate adder circuits.

Keywords: Carry Select Adder, Efficient Approximation, Power consumption, Error Tolerance, Image addition

1 Introduction

With the widespread use of VLSI architectures in digital signal processing Systems, the circuit complexity and the amount of data processed by the circuits are increasing rapidly. This poses a major bottleneck for battery operated electronic devices in terms of achieving desired performance and lesser entire power consumption at the identical moment. Adders form a vital part of digital filters on which the performance of a DSP system depends upon.

A wide range of signal processing applications is highly error tolerant. A certain degree of errors in the results does not affect the quality in which the results [1, 2] are sensed by the humans. Approximate addition technique exploits this feature and aims to achieve less vicinity, power and high-speed with fine-tuned accuracy in signal processing applications [3, 4].

In this work, an approximation technique for adders is proposed to attain optimal performance based on area, speed and entire power while keeping the error low [5] and verified through hardware implementation in image processing applications [6]. Our paper is organized as follows Section 2 describes the conventional adder theory, Section 3 describes the proposed efficient approximate full adder, implementation of the proposed adder in adder topology of carry select adder and its analysis, Section 4 deals with the result and discussion, Section 5 gives a picture of the conclusion of the paper.

2 Existing Conventional and Exact Adder Theory

2.1 16-bit Conventional CSLA

An adder is a digital path that acts upon expansion of numbers. In numerous PCs and different sorts of processors, adders are utilized in the math rationale units or ALU. It may be developed very well for some number portrayals, for example, excess-3; the most widely recognized adders works on binary numbers. Based on bit

* Corresponding author e-mail: nishokvs@mail.com

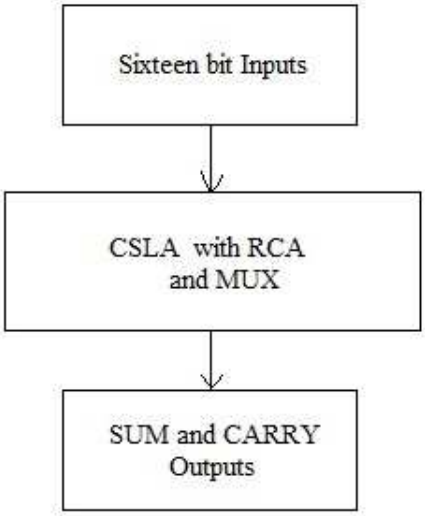

Fig. 1: 16-bit Conventional CSLA

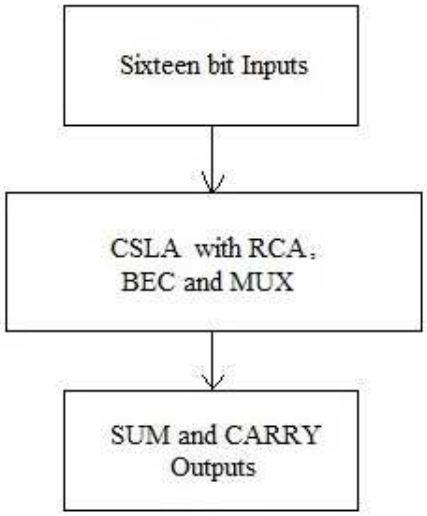

Fig. 2: 16-bit Exact CSLA

types, adders are classified into half adder (two-bit), full adder (three-bit); ripple carry, carry save, carry select and square root carry select are adders with multiple bits. The swiftness of the adder is determined by how quick the carry can pass/pre-calculated.

By make use of carry ripple adders and a multiplexer, the structure of carry select adder is built. This adder circuit is simple but attains faster results with great accuracy. In this type of adders, the addition of two n-bit values is done parallel with two carry ripple adders, using $C_{\text{in}} = 0$ and $C_{\text{in}} = 1$ carry input respectively. Output from both ripple carry adders are given as input to a multiplexer that provides the final output based on the control signal. If the C_{in} is 0, the output is selected from upper ripple carry adder and if $C_{\text{in}} = 1$, the output is selected from lower-order ripple carry adder [7]. This kind of calculation keeps away the issue of carry propagation delays in CSLA and performs the calculations 40% and above faster than the normal Ripple carry adder [8]. As the truth table and k-map minimization are discussed before several times, the block diagram of the carry select adder is shown in Fig. 1

2.2 16-bit Exact CSLA

In lots of arithmetic calculations, the carry select adder is employed to generate multiple carries self-sufficiently and then pick a carry to produce the sum value that lightens the propagation delay issues [7]. Using multiple duos of Carry Ripple Adders (RCA) to produce partial sum and carry with $C_{\text{in}} = 0$ and $C_{\text{in}} = 1$ alternatively increases the stay and thus diminishes the overall efficiency. The exact CSLA follows basic idea of using Excess-1 Converter (BEC) as a replacement for carry

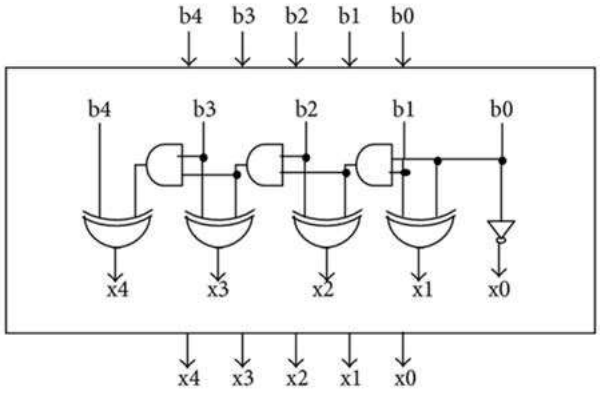

Fig. 3: 5-bit circuit of BEC

ripple adder with $C_{\text{in}} = 1$ in the conventional carry select adder to achieve hardware simplicity and better utilization of power [9]. Carry select adder is made known in Fig. 2 The logic BEC of $n + 1$-bit utilizes fewer logic gates when compared to n-bit Full Adder.

The outputs from RCA and BEC logic are given as inputs to a respective multiplexer which select and give the final sum based on the control signal C_{in} [10]. Similarly, the calculation takes place in remaining full adder cells and thus produce sum and carry out results of exact CSLA. A circuit of BEC of 5-bit and its practical chart are displayed in Fig. 3 and Table 1 respectively.

The Boolean expressions for the design of the 5-bit BEC is listed as (note the functional symbols $\sim$, NOT, & AND, $\wedge$ XOR)

Table 1: 5-bit BEC Practical Table

B [4:0]	X[4:0]
00000	00001
00001	00010
...	...
11110	11111
11111	00000

X0 =∼ B0
X1 = B0 ∧ B1
X2 = B2 ∧ (B0 & B1)
X3 = B3 ∧ (B0 & B1 & B2)
X4 = B4 ∧ (B0 & B1 & B2 & B3)
The 464 gate count of 16-bit exact CSLA reveals that the circuit is simplified 22% compared to the conventional CSLA.

For larger *n*-bit designs, with the higher performance, the exact CSLA is used for enhanced results.

3 Proposed EA CSLA Adders

3.1 Efficient Approximation Full Adder

This section explains the proposed Efficient Approximation CSLA (EA-CSLA) in detail. In conventional and exact carry select adders, even though two parallel-carry ripple adders are utilized to execute fast calculations, waiting time of present input for the previous output gives way to the propagation delay and the carry path delay. These delays increase the processing time and further reduces the speed of the circuit.

The existing error tolerant adders solve these issues and perform the addition in speed manner. But the output varies much from accurate results and thus creates accuracy issue for larger *n*-bit calculations [11].

In this paper, two efficient approximation full adders are proposed. In the proposed EAI full adder, a new concept is accessible that bring in errors in two sum terms and in one carry term. Likewise, the proposed EAII full adder brings in errors in two carry terms. Those errors result in nearly-varied sum outputs and accuracy which is acceptable in range. The benefit of this concept is lessening the paths and gates in full adder circuitry [12, 13]. Consequently, the adder performance is enhanced in contrast to error tolerant and existing approximation adder.

Table 2 shows the proposed efficient approximation I CSLA truth table from which the k-map minimization takes place for the logic implementation of proposed EAI approximation full adder circuit and displayed in Fig. 4 and Fig. 5, respectively.

Table 3 shows the truth table of proposed EAII-CSLA from which the k-map minimization takes place for the logic implementation of proposed EAII full adder circuit and displayed below in Fig. 6 and Fig. 7, respectively.

Table 2: Truth table for EAI full adder

Inputs Bits			Outputs Bits	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1(Error)	0(Error)
1	0	0	0(Error)	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

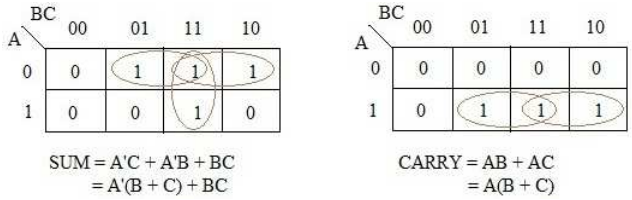

Fig. 4: EAI full adder minimization by K-map

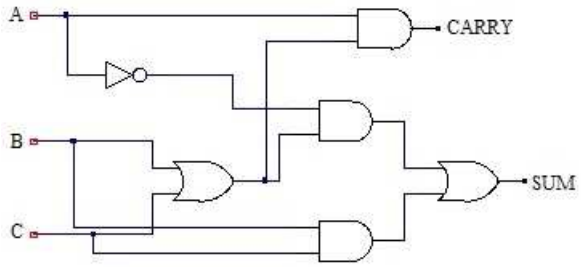

Fig. 5: EAI full adder Logic Implementation unit

Table 3: Truth table for EAII full adder

Inputs Bits			Outputs Bits	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1(Error)
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0(Error)
1	1	0	0	1
1	1	1	1	1

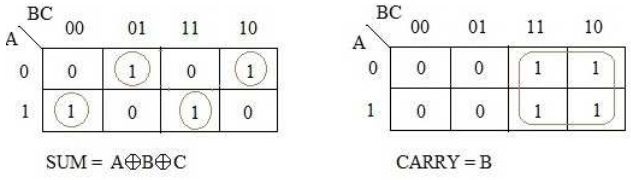

Fig. 6: EAII full adder minimization by K-map

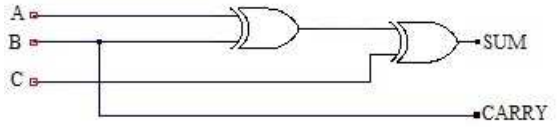

Fig. 7: EAII full adder Logic Implementation unit

3.2 Proposed Efficient Approximation 16-bit CSLA

In the proposed 16-bit size EA-CSLA, the algorithmic split-up technique is utilized which diminish the waiting time in all path of the circuit. In this EA-CSLA, the bit size of 16 is first partitioned into accurate part and inaccurate part with each part containing 8-bit and those 8-bits are further subpartitioned into 4-bit parts. This 4-bit split-up technique diminishes the path delay and results in high-performance outcomes. Block diagram of the proposed efficient approximation Carry Select Adder is displayed in Fig. 8 The 8-bit accurate part is of accurate full adder performs normal addition and the inaccurate part performs proposed approximation-based addition [14, 15].

The inaccurate part utilizes a lesser number of gates than the accurate part. The proposed EAI attains 33% less area and EAII attains 40% less area than conventional CSLA, respectively. The structure of proposed efficient approximation carry select adder is displayed below in Fig. 9.

The below equations used in error analysis as follows:
Error distance of designs $= |S' - S|$
where S' is approximate sum and S is accurate sum.

Let the two random input variables be 5870 and 2669. The accurate sum (S) with $C_{\text{in}} = 1$ obtained be 8540. The approximate sum (S') from the proposed 16-bit EAI-CSLA with $C_{\text{in}} = 1$ is 8537.

Thus the error distance for given two random variables can be calculated as follows:

$$\text{Error Distance } (ED) = |8537 - 8540| = 3$$

$$\text{Relative Error Distance of designs} = \frac{\text{Error Distance } (ED)}{\text{Accurate Sum } (S)}$$

$$= 3/8540$$

$$= 0.000351$$

Table 4: Performance comparison of adders

Adder	Area (LUTs)	Delay (ns)	Power (mW)	PDP (pJ)
Conventional CSLA	66	24.597	190.40	4683.8
Exact CSLA	54	18.618	186.47	3472.1
Proposed EAI-CSLA	44	18.026	179.05	3227.5
Proposed EAII-CSLA	39	16.334	180.59	2949.0

Consequently, the error percentage is calculated using the below equation.

$$\text{Percentage of error} = [(S - S')/S] \times 100$$

$$= [(8540 - 8537)/8540] \times 100$$

$$= 0.035$$

The error percentage of given two random-input variables is 0.035. Likewise, by considering all possible 2^{16} input combinations, outputs and error analysis outcomes are obtained.

4 Results and Discussion

The proposed EA of 16-bit size has been developed using Verilog language. Analyzed and synthesized in Altera Quartus II and in Encounter-Cadence 90 nm synthesis tool. The conventional, exact, existing, EAI and EAII CSLA adders are simulated with 16-bit and their performance outcomes are tabulated below. Table 4 exhibits the comparison of adders based on the area, delay, power, and PDP synthesized in Altera Quartus II. The delay reveals the decrease based on hardware simplicity in proposed EAI and EAII CSLA adders with reduced power consumption. EAI performs 27% fast calculations than conventional and 3.2% than exact adders; EAII performs 34% fast calculations than conventional and 12.3% than exact adders respectively.

Table 5 displays the comparison of adders based on the area, delay and power synthesized in Cadence Encounter RTL compiler. EAI utilizes 37% fewer power than conventional and 32% than exact adders, EAII utilizes 32% fewer than conventional and 27% than exact adders respectively. The reduction in power consumption than existing SAET-CSLA shows the less waiting time in carry path and the hardware simplicity of the proposed circuits [16].

Table 6 exhibits the error analysis based on input and output values of adders with $C_{\text{in}} = 0$. Error analysis displays the error of both EA adder outputs which is very least and indicates that the proposed circuits can be utilized for all error-tolerant applications.

In addition, the proposed system hardware implementation is done and verified through system generator and the device Xilinx Spartan 6 XSLX4T

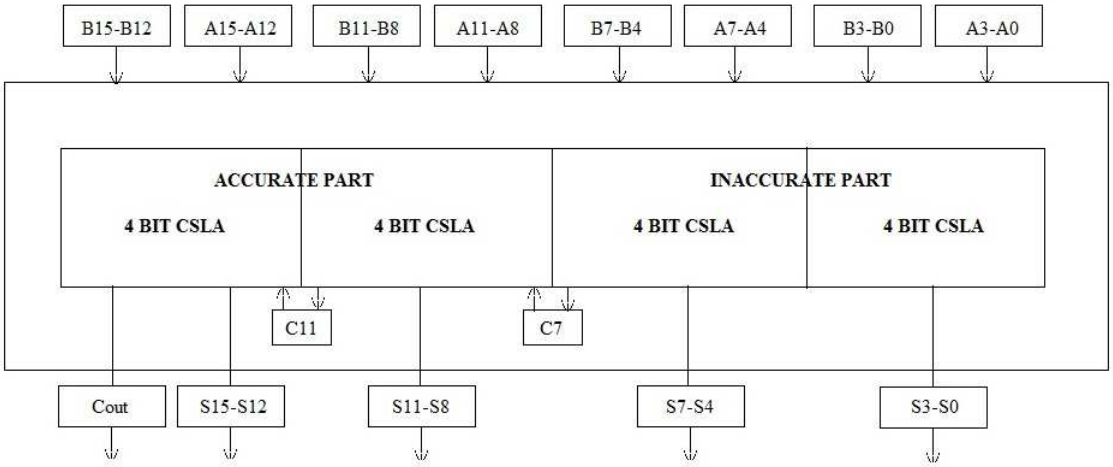

Fig. 8: 16-bit Proposed EA-CSLA

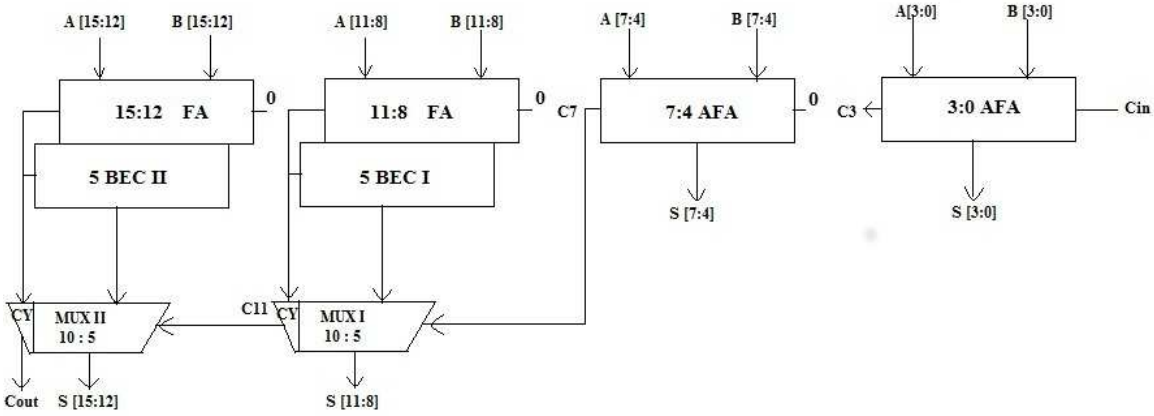

Fig. 9: 16-bit proposed EA-CSLA structure

Table 5: Performance comparison of adders

Adder	Area (LUTs)	Delay (ps)	Power based on cell Leakage (nW)	Power based on circuit usage and wire (nW)	Entire Power (nW)	Delay × Entire Power (fJ)
Conventional CSLA	48	1479	3509.6	30603.9	34113.5	50.455
Exact CSLA with BEC	58	1566	3080.5	28415.0	31495.5	49.323
Existing SAET-CSLA	48	1329	2706.3	27462.1	30168.4	40.093
Proposed EAI-CSLA	46	1163	2143.6	19476.2	21619.8	25.143
Proposed EAII-CSLA	44	1109	2446.7	20650.9	23097.6	25.615

CSG324 is used. The images of the same size (256 × 256) are added through our proposed EAI-CSLA design. The architecture of image addition and the input and outputs with hardware implementation kit are shown in Figs. 10 and 11 respectively.

5 Conclusions

Efficient approximation CSLA adder has designed and its performance establishes with less waiting time in carry path and hardware simplicity. The above outcomes are

Table 6: Error analysis of proposed EA-CSLA for 16-bit size

R.No	Input Value		Sum		Percentage of Error in EAI adder	Sum	Percentage of Error in EAII adder
	I	II	Conventional Carry select adder	Proposed EAI Carry select adder		Proposed EAII Carry select adder	
1	5870	2669	8539	8537	0.023	8265	3.209
2	10861	7623	18484	18322	0.876	18468	0.087
3	10900	21859	32759	32611	0.452	32561	0.604
4	22997	27876	50873	50856	0.033	50937	0.126
5	30439	40553	70992	70984	0.011	70948	0.061
6	32117	36561	68678	68656	0.032	68614	0.093

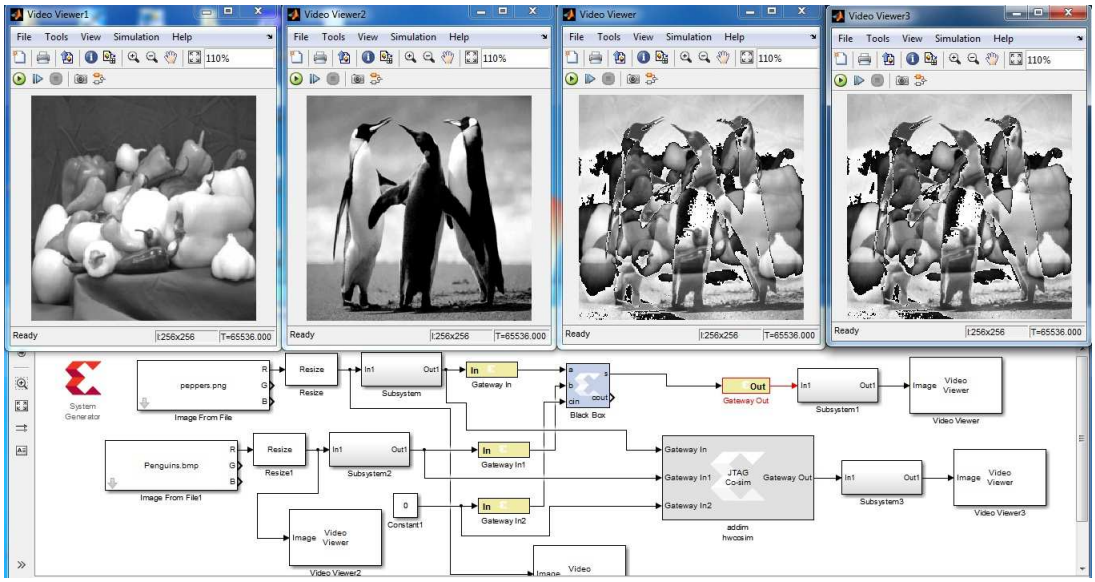

Fig. 10: The architecture of proposed design with input and its output through Xilinx system generator with Simulink and FPGA device

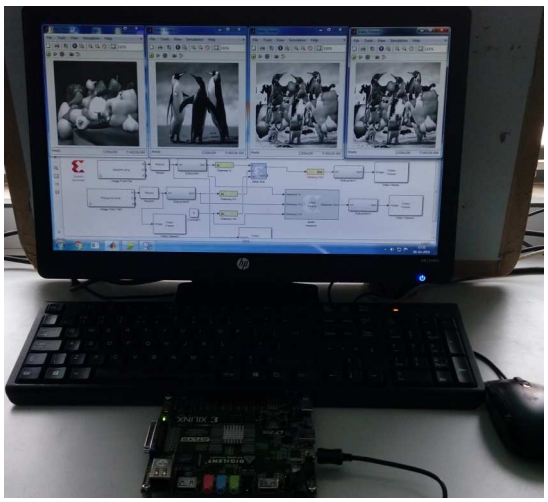

Fig. 11: Hardware implementation using Xilinx Spartan 6 csg324 device

evidence for that the EA CSLA adder testimony efficient lessening in area and path delay compared to the accurate and exact CSLA respectively. From our 2^{16} inputs, error analysis figures just about 0.74% for EAI and 1.22% for EAII with not as much of power consumption. This error can be more dropped by fresh EA adder types. Consequently, with less leakage and utilization power, proposed EA CSLA adders are capable of implementing further in error-tolerant image and signal processing applications. By way of the above design and analysis, implementation in image addition application is conceded.

References

[1] N. Zhu, W.L. Goh, K.S. Yeo, An enhanced low-power high-speed adder for the error-tolerant application. Proc. IEEE Int. Symp. Integrn. Circuits, pp. 69–72 (2009).

[2] A.N. Jayanthi, C.S. Ravichandran, Design of error-tolerant adder, Am. J. Appl. Sci., vol. 9, no. 6, pp. 818–824 (2012).

[3] B. Ramkumar, M. Harish, Low-power and area-efficient carry select adder, IEEE Trans Very Large Scale Integrn Sys., vol. 20, no. 2, pp. 371–375 (2012).

[4] Y. Kim, L.S. Kim, 64-bit carry-select adder with reduced area, Electron. Lett., vol. 37, no. 10, pp. 614–615 (2001).

[5] O. Vignesh, H. Mangalam, K. AnjuBala, Survey on Approximate multipliers for image processing, Eurpn. Jrnl. Adv. in Engg. and Tech., vol. 5, no. 5, pp. 344–349, (2018)

[6] O. Vignesh, H. Mangalam, S. Gayathri, FPGA Architecture for text extraction from images, Clstr. Comptng, The Jrnl. of Networks, Software Tools and Applns., vol. 21, pp. 1–10, (2018)

[7] O.J. Bedrij, Carry-select adder, IRE Trans. Electron. Comput., pp. 340–344 (1962).

[8] R. Jothin, C. Vasanthanayaki, High-performance significance approximation error-tolerance adder for image processing applications, J. Electron Test., vol. 32, no. 3, pp. 377–383 (2016).

[9] B. Ramkumar, H.M. Kittur, and P.M. Kannan, ASIC implementation of modified faster carry save adder, Eur. J. Sci. Res., vol. 42, no. 1, pp. 53–58 (2010).

[10] P. Saxena, U. Purohit, P. Joshi, Analysis of low power, area efficient and high-speed fast adder, Int J Adv Res Comput Commun Eng., vol. 2, no. 9, pp. 356–375 (2013).

[11] S. Singh, D. Kumar, Design of area and power efficient modified carry select adder, Int. J. Comput. Appl., vol. 33, no. 3, pp. 975–987 (2011).

[12] V. Muralidharan, M. Jagadeeswari, An enhanced Carry elimination adder for low power VLSI applications, Int. J. Eng Res Appl., vol. 2, no. 2, pp. 1477–1482 (2012).

[13] S.L. Lu, Speeding up processing with approximation circuits, IEEE Computer., vol. 37, no. 3, pp. 67–73 (2004).

[14] R. Sakthivel, H.M. Kittur, Energy efficient low area error tolerant adder with higher accuracy, Circuits, Systems, and Signal Processing, vol. 33, no. 8, pp. 2625–2641, (2014).

[15] V. Gupta, D. Mohapatra, S.P. Park, A. Raghunathan, K. Roy, IMPACT: imprecise adders for low-power approximate computing, Proc IEEE/ACM Int Symp Low-Power Electron Des., pp. 409–414 (2011).

[16] K.K. Parhi, VLSI digital signal processing systems: design and implementation, pp. 255–279, Wiley (2007).

V. S. Nishok is currently a Research Scholar in the Department of Electronics and Communication Engineering, KalaignarKarunanidhi Institute of Technology, Tamil Nadu, India. He obtained M. E., from Anna University, Coimbatore, in the discipline of Master of VLSI design in the year of 2011. He has 5 years of teaching experience at UG and PG levels. His fields of interests include Low Power VLSI, Signal Processing & Image Processing.

P. Poongodi is currently working as Professor in the Department of Electronics and Communication Engineering, KalaignarKarunanidhi Institute of Technology, Tamil Nadu, India. She obtained M.E., from Bharathiar University, Coimbatore, in the discipline of Master of Applied Electronics in the year of 1994. She obtained her PhD in the area of Control System in the faculty of Information and Communication from Anna University, Chennai, in the year 2006. She has more teaching experience at UG and PG levels, also guiding many PhDs in the area of Electronics and Communication Engineering. Her fields of interests include Soft computing, Computer Communication and VLSI design.

K. N. Vijeyakumar is currently working as Associate Professor in the Department of Electronics and Communication Engineering, Dr. Mahalingam College of Engineering and Technology, Tamil Nadu, India. He obtained M.E., from Anna University, Chennai, in the discipline of Master of Applied Electronics in the year of 2007. He obtained his PhD in the area of VLSI in the faculty of Information and Communication from Anna University, Chennai, in the year 2013. He has more teaching experience and guiding many PhDs in the area of Electronics and Communication Engineering. His fields of interests are ASIC design, VLSI design, Digital system design, and Embedded system design.