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A New Processing Method for Signal and Image Analysis Using Discrete Wavelet Transform

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Abstract: In this paper, we develop a new method for the analysis of signal and image data using Discrete Wavelet Transform (DWT). The new method reduces the size of the computing devices and consumes less energy. Out of different transformation techniques, the most famous and dominant architecture is the discrete wavelet transform. The discrete wavelet transform design optimization has done on power and leakage current reduction. New adders are proposed which are based on power gating and reversible logic. It is shown that the proposed adders reduce the dynamic power by about 30%. The proposed design in 45 nm and 32 nm CMOS technology is efficient when compared to other methods.

Keywords: Adder, CMOS, DWT architecture, Leakage reduction, Low power, MAC, Multiplier.

1 Introduction

The ultra low-power design for wavelet transform is an emerging technology under very large scale integration (VLSI) [1]. In speech and image processing applications the signal input is non stationary and transformation into time or frequency form architecture is used. Among several transformation techniques, the wavelet transform stands speed due to its time scale analysis of the input signal [2]. In the literature, VLSI architecture is used as a wavelet transform architecture. The structure of wavelet transform filters bank consists of low pass and high pass filter. To reduce the power consumption of any electronic device, the arithmetic and logic unit (ALU) should be optimized in terms of power consumption [3]. The performance can be improved by enhancing architecture, processing style or algorithm. The different enhancement schemes are distributed arithmetic techniques, parallel distributed arithmetic, retiming, folding, and so forth. etc. The parallel distributed arithmetic methods increase speed but also increase the number of replications or components For the reduction of critical paths retiming, folding and flipping architectures are utilized [4].

The presence of the multiplier unit in the ALU increases the power consumption. Aradhana Uniyal [5] proposed an ALU which can perform eight arithmetic and logical functions. The optimized adder structure uses the theory of transition logic element. The gate voltage is controlled to reduce peak current in the load. Negative Differential Resistance (NDR) circuit [6] is used in full adder design for current efficiency but it is complicated in design. The conventional adders like Carry Select Adder are used in data processing applications. The Manchester carry chain (MCC) improves the speed of the arithmetic operations [7]. The power-delay product is low when multi output circuits like domino logics are designed using Manchester carry chain blocks.

The signal from the input end is difficult to process. After suitable processing, the transformation is applied on the input signals. To perform the signal processing, Digital Signal Processing (DSP) architectures are designed. The low-power and high-speed adders are to be used in multipliers. The Dadda multiplier is implemented using pass-transistor logic to reduce the power-delay product [8]. A hybrid adder is designed using pass and transmission gates to improve the power dissipation and output voltage [9, 10].

The Vedic mathematics-based adders consume less power but have larger area and larger power-delay product. The full adders are designed using XOR and multiplexer [11] which provides low power-delay and moderate area occupancy. The two CMOS gate-based

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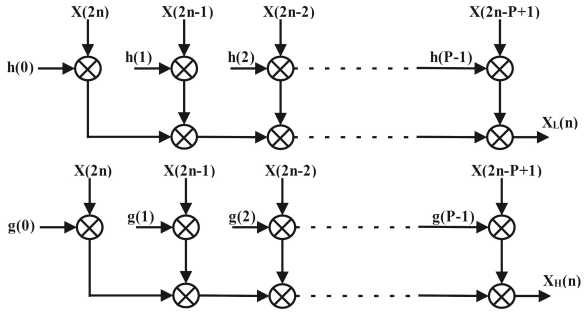

Fig. 1: General convolution-based architecture

topologies minimize the area used. The compressor-based [12] adders consume less power but lower the accuracy. The carry prediction overcomes the approximation in compressor adders and conventional adders [13]. The error detection/correction circuitry for adders is used in pipelining which improves the performance. A Quantum-dot Cellular Automata (QCA) decimal full adder is presented in literature [14]. Aside from individual adders, hybrid adders are designed in [15, 16]. The fast adders enhance the overall performance of the Vedic multiplier. The comparative analysis is done with RCA in literature [17]. The combination of the carry-lookahead and carry-select adder architecture with a 16-bit word length is designed and proves to be more efficient. Radiation hardened low power magnetic full-adder [18] improves the ALU performance with overhead on design complexity. In-exact computing methods use compressors structures for video coding units [19]. Few adders are designed using optical domain switches with reversible functionality to reduce the delay and cost [20].

This paper is organized as follows: In Section 1, an introduction is presented followed by literature survey in Section 2. In Section 3, background methods are presented. In Section 4, the proposed method is presented. The results and discussion are presented in Section 5. The conclusion is presented in Section 6.

2 Architecture of DWT

For the analysis of signal and image data, Discrete Wavelet Transforms (DWT) is considered a powerful tool. Various types of architecture have been developed for DWT signal processing. The different types of structures for DWT architecture are direct form, poly phase, lattice and lifting structure. The convolution-based DWT method [21] uses Finite Impulse Response filters (FIR) to design the high pass and low-pass design. The folded architectures are [22] broadly classified into serial and parallel architectures. The other techniques used for the filter design are filter bank structure, digit serial pipelining, poly phase decomposition and coefficient folding technique. The convolution-based DWT architecture which is shown in Fig. 1 occupies more area and consists of processing elements like multipliers and adders. The lifting-based architecture relies on the spatial domain and is more advantageous when compared to convolution filer bank structure as it uses fewer number of processing elements. [23].

Other advantages are:less area, reduced power consumption and less computational complexity [24]. The simpler computation helps in implementing the architecture in FPGA and ASICs [25]. But since FPGAs suffer from flexibility issues, circuit level customization is more advantageous. The integer-to-integer lifting-based wavelet transforms are widely used in lossless coding and JPEG. Fig. 2 shows the lifting scheme wavelets filter which consists of Split step (S), Predict step (P), and Update step (U). The input samples are divided into even and odd points in split step and multiplied by the predict factor in predict step. The detailed coefficients (dj) are generated using high pass filtering. In Update step, the predict step output is multiplied by the update factors. The coarser coefficients are obtained through low pass filtering [26].

The basic functional units of the lifting-based schemes are given in Fig. 3. It is noted from Fig. 3 that the basic elements or functional units of the lifting-based scheme contain adders, multipliers and delay elements. The lifting-based schemes need memory elements to store the predict and update information.

3 Background Methodology

Compared to the convolution-based DWT architecture, the lifting-based architecture is computationally simpler and faster. Only the memory requirements are little more. In this work a direct mapped architecture for a lifting-based DWT system is designed with the proposed Multiply and accumulation (MAC) design. This design is effective on the basis of power, delay and area. From Fig. 4 it can be observed that the architecture is built with multipliers, adders, and delay elements. The delay element is a flip flop or a latch which depends on the clock requirements. For shared architecture, a multiplexer is used to choose between the coefficients of LPF and HPF. The decomposition level takes place in the block for multiple co-efficient. The adder is one of the most critical and important components in a processor core, because it is the part of the multiplier or MAC unit in the processor core. In dedicated circuits like CORDIC, Transforms, etc., adder consumes most of the computing time and power. The full adder logic function for sum and carry can also be written as

$$SUM = A\bar{\oplus}B\bar{\oplus}CIN \tag{1}$$

$$COUT = (A \wedge (A\bar{\oplus}B)) \vee (CIN \wedge (A \oplus B)) \tag{2}$$

The conventional CMOS adder is shown in Fig. 5 has 58 Transistors which is bulky. Full adder of energy recovery logic uses only 10 transistors and consumes less power as

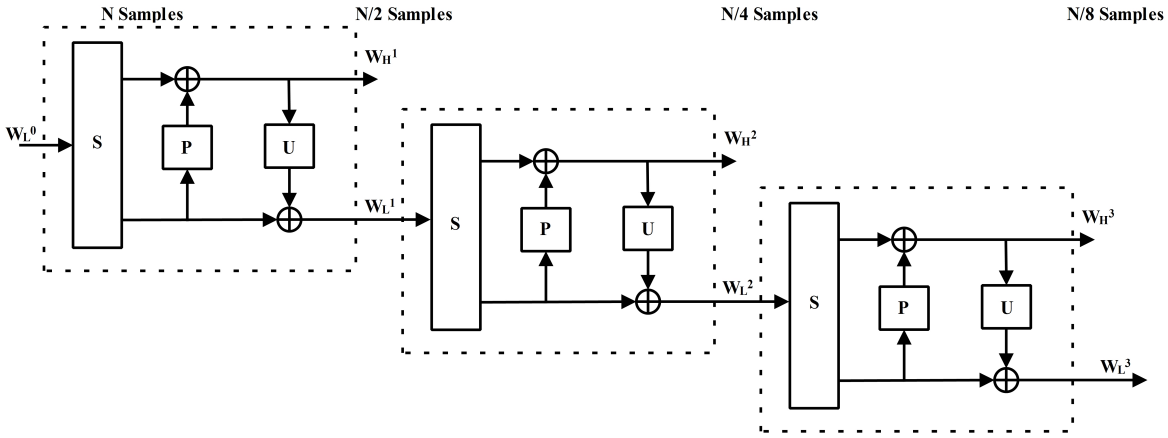

Fig. 2: Block Diagram of the lifting-based scheme with split unit (S), update unit (U) and predict block (P)

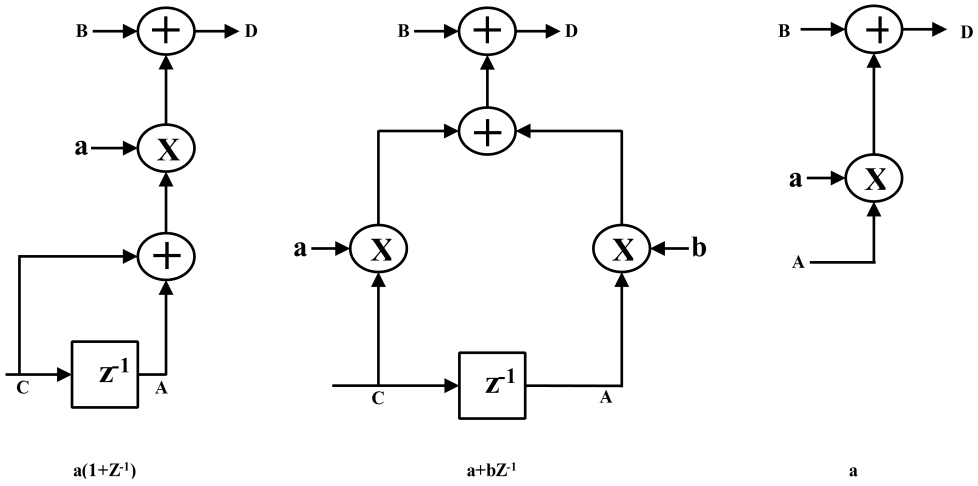

Fig. 3: Basic functional units ((+)-adder, (×)-multiplier) of lifting-based DWT architecture for split unit, update unit and predict unit

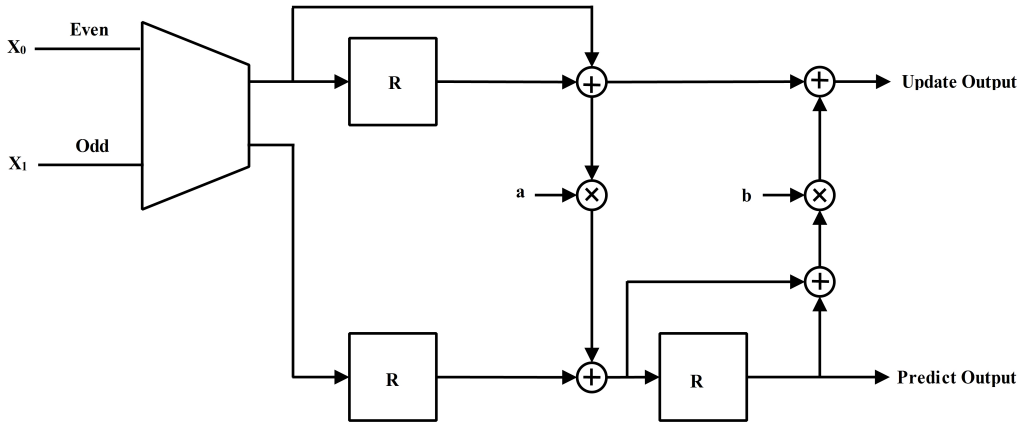

Fig. 4: Block diagram of the lifting-based direct mapped architecture

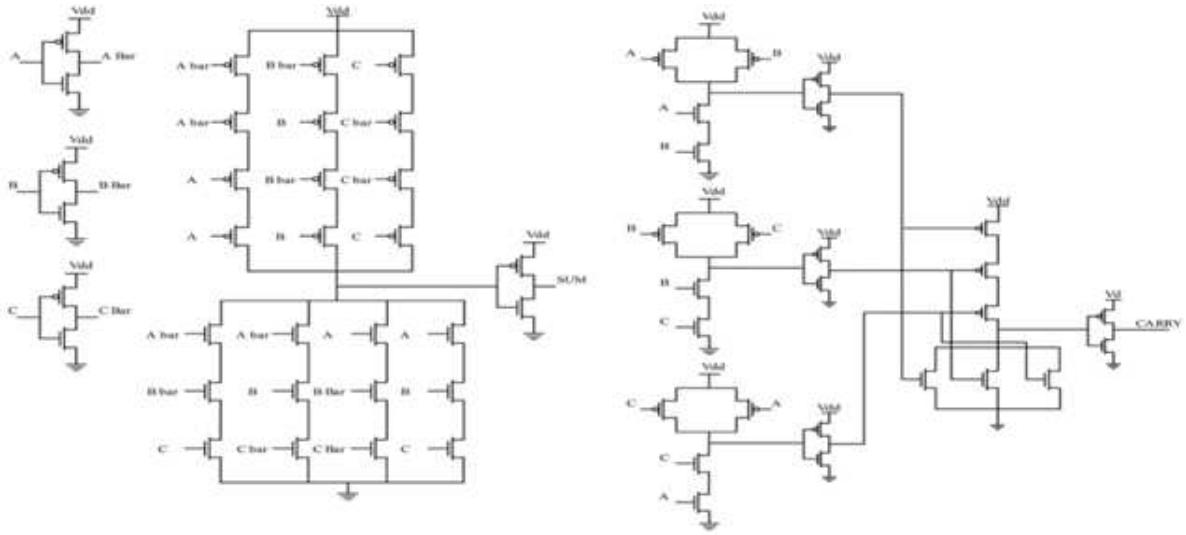

Fig. 5: Circuit of the conventional adder for processor core architecture

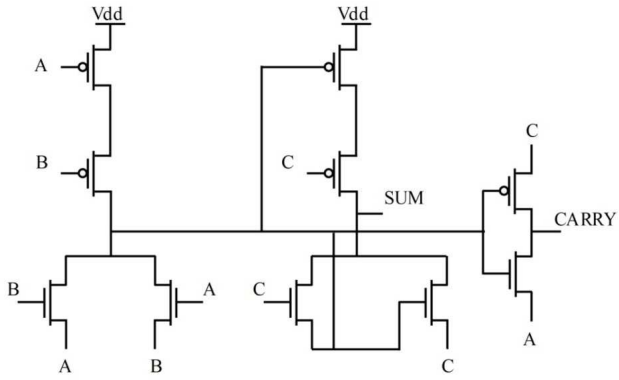

Fig. 6: Circuit diagram of the existing energy recovery adder

shown in Fig. 6. The adder uses a set of XOR–XNOR gates and the frequency of operation is higher which is suitable for the DWT system. The performance of the multiplier with the adder is promising.

4 Proposed Method

The direct mapped lifting-based DWT can be easily optimized to achieve better speed than other types. The direct form has simpler computation which helps in designing and implementing the architecture in FPGA and ASICs. Power gating reduces the power by shutting off the power to the circuit which is not in use based on the data. This also reduces the stand-by or leakage power. Obviously, the number of components increases but the overall power will be reduced with an additional delay. Power gating uses PMOS and NMOS transistors for header and sleep transistors respectively.

The proposed circuit for performing addition operation is shown in Fig. 7 and 8. The circuit is based on an XOR gate and a multiplexer with the power gating on power supply. The individual blocks are based on CMOS technology. The input 'B' and carry input (C_{in}) are given to the XOR module. The output of the XOR module is inverted and buffered with power gating. The gated buffer output is given to one end of the multiplexer MUX1, whose other end is connected with the output of the XOR module directly. The input 'A' is connected with selected line of MUX1 which chooses between the XOR module output and its power gated inverse. This forms the sum output. The MUX2 block is connected with the inputs A and C_{in}. The XOR output selects between two inputs and produces the carry output (C_{out}). The design of inverter 'b1' is typical. The W/L ratio for PMOS transistor M_2 is made twice than that of M_1. The M_1 and M_2 transistors form the power gated unit, which connects the power supply VDD with buffer b1 or b2, when the value of A for power gating is 1 for NMOS and 0 for PMOS transistor. For the off case of M_1 and M2, the power is saved for four cycles. The circuit with PMOS power gating consumes less power when compared to NMOS power gating. The XOR module in Figs. 7 and 8 occupies two transistors. The two multiplexers (MUX1 and MUX2) is shown in Figs. 7 and 8, occupy two transistors each. So the total transistors used for the design is nine. The reversible logic circuits are acyclic (functions in forward and backward directions) as shown in Fig. 9. It has no fan-out. A unique output pattern is produced for every input pattern and inputs can be generated from outputs through reversible computations. So a one-toone physical reversibility reduces Energy dissipation. 32 nm and 45 nm technologies are used for simulation, but below 32 nm is not advisable for the design with CMOS circuits.

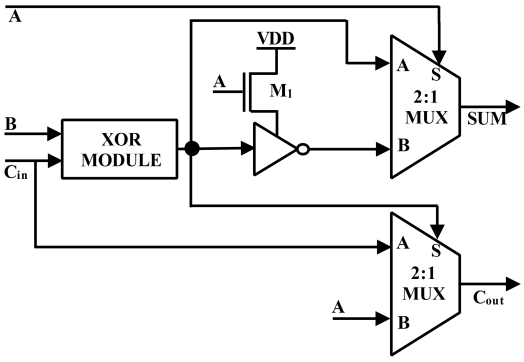

Fig. 7: Circuit diagram of the proposed adder with n-power gating

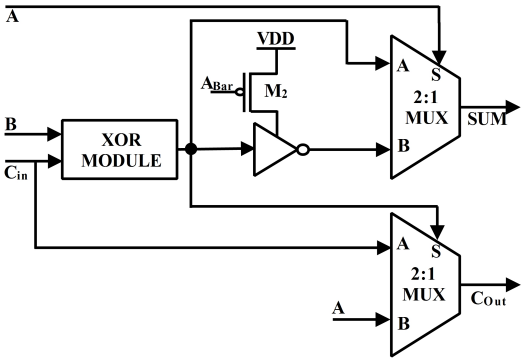

Fig. 8: Circuit diagram of the proposed adder with p-power gating

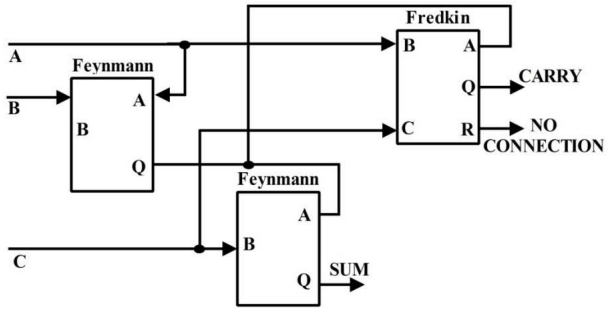

Fig. 9: Circuit diagram of the proposed reversible adder

The proposed adders are used to design the multiplier unit for MAC block in the DWT architecture. The proposed multiplier on which the adders are used are shown in Figs. 10 and 11. In Figs. 10 and 11, the adder blocks are replaced with the proposed adders and the performance is investigated. As the multiplier unit forms the critical element in the overall design, reducing the power consumption of the multiplier is the priority.

5 Result and Discussion

The performance of the proposed adders and existing adders are tabulated in Tables 1 and 2. The proposed adders are compared with the adder types: 12 Transistor adder, 20 Transistor adder and 28 Transistor adder. The power, area and energy are measured. The results show that the proposed adder improves the power consumption by about 68% with 12T adder, 74% with 20T adder and 80% with 28T adder and so on.

The proposed N-Power gating, P-Power gating and reversible logic adders consume less power than the conventional adders like 12T, 20T and 28T adders.

Among the three proposed adders, the reversible adder provides better results than the other two. The proposed reversible adder is 54% and 55% more power efficient than the N-Power gating and P-Power gating based adders respectively. The multipliers are designed using all the three proposed adders. Here, three multipliers are considered for comparison such as, Array multiplier, Bough wooly multiplier and Braun multiplier. Results are tabulated in Tables 3 and 4.

For the comparison process, all the multipliers are designed in 32 nm and 45 nm technology. The performance of the MAC circuits is tabulated in Tables 5 and 6 for conventional and proposed multipliers. The total number of multipliers required to implement the chosen MAC architecture for DWT is 1.

So, for a single multiplier block, a 75% and 33% of power is reduced when compared to a conventional method for 32 nm and 45 nm respectively. This collective improvement will reduce the buffering usage and long term working of the system. From the all above analysis, it can be concluded that the proposed MAC circuit with the proposed adders for DWT architecture are efficient when compared to the conventional methods. The objective of this work is to design a new processing unit. The MAC unit for the DWT architecture is designed with low power circuits. Below 32 nm, the CMOS technology suffers from the small channel effects and other second order problems. The work will be expanded in designing the circuits in multi gate devices.

6 Conclusion

In this work, a new processing element is designed for the DWT architecture. The power consumption of the computing components is kept small and energy consumption is lowered. The proposed methods are compared with existing circuits. The performance shows that the proposed method consumes less power compared to the existing methods. The basic building block of the DWT architecture is the multiplier and it is optimized by all parameters. In this paper the optimization is done on the power consumption in the adders by proposing the power gating technique. The work is extended towards designing an adder using reversible logic. The proposed

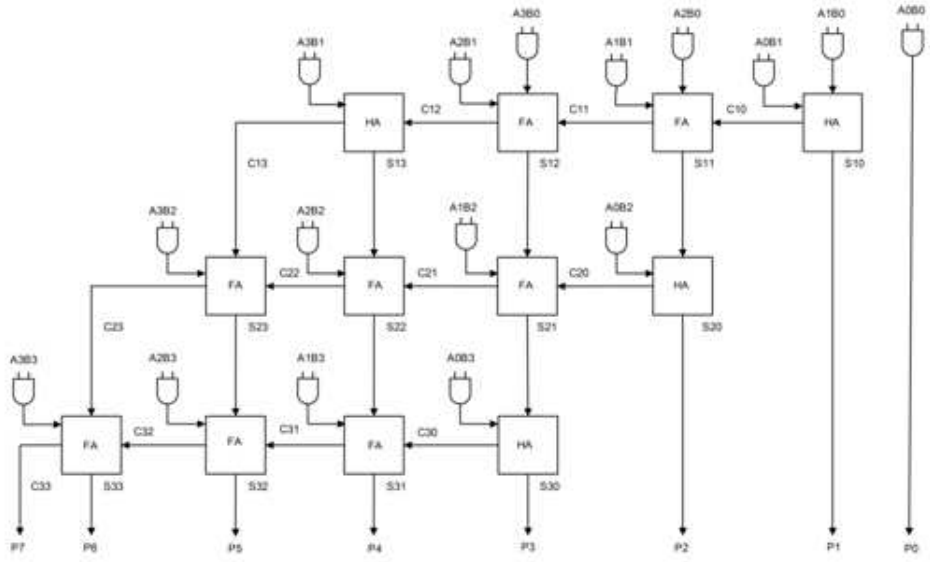

Fig. 10: Circuit diagram of the proposed 4 bit array multiplier

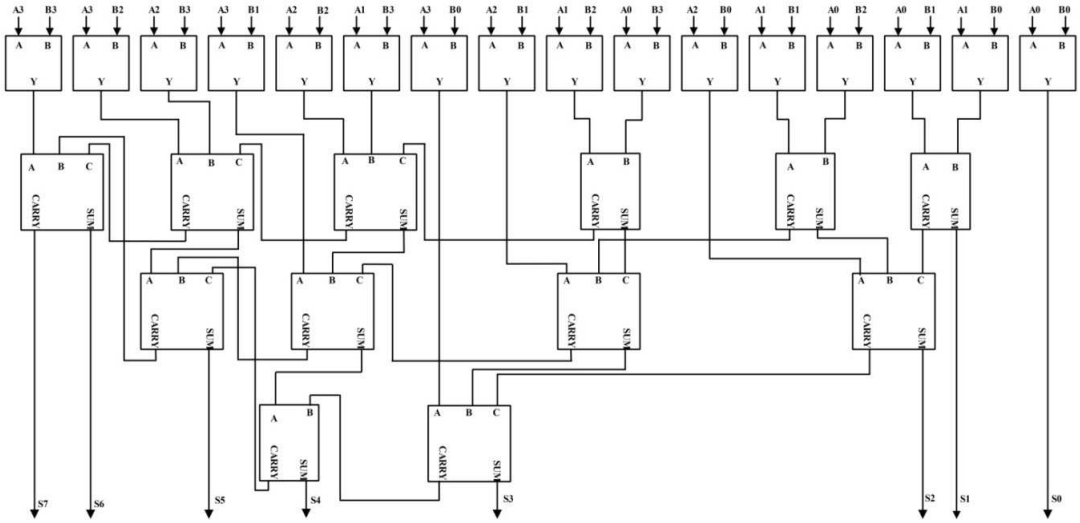

Fig. 11: Circuit diagram of the proposed reversible adder based multiplier

Table 1: Comparison between power consumption of adders using 32 nm. *—Existing Adder, & —Proposed adder

Name of the circuit	Power (W)	Average current (A)	Average power (W)
12 Transistor Adder*	83.46×10^{-09}	45.88×10^{-09}	45.67×10^{-09}
20 Transistor Adder*	7.61×10^{-06}	53.36×10^{-09}	46.24×10^{-09}
28 Transistor Adder*	219.38×10^{-09}	166.36×10^{-09}	166.11×10^{-09}
N-Power Gating adder &	142.40×10^{-09}	27.14×10^{-09}	2.62×10^{-09}
P-Power Gating adder &	142.72×10^{-09}	27.146×10^{-09}	2.625×10^{-09}
Reversible adder &	214×10^{-09}	99.42×10^{-09}	87.27×10^{-15}

Table 2: Comparison between power consumption of adders using 45 nm

Name of the circuit	Power (W)	Average current (A)	Average power (W)
12 Transistor Adder	35.88×10^{-09}	33.12×10^{-09}	32.88×10^{-09}
20 Transistor Adder	3.79×10^{-06}	2.11×10^{-09}	1.81×10^{-09}
28 Transistor Adder	38.17×10^{-09}	36.07×10^{-09}	36.03×10^{-09}
N-Power Gating adder	12.78×10^{-09}	1.07×10^{-09}	81.56×10^{-12}
P-Power Gating adder	12.79×10^{-09}	1.07×10^{-09}	81.56×10^{-12}
Reversible adder	34.77×10^{-09}	33.70×10^{-09}	3.76×10^{-15}

Table 3: Comparison between power consumption of proposed multipliers using 32 nm

Name of the circuit	Name of the circuit	Average current (A)	Average power (W)
Array multiplier	Multiplier with n-power gating adder	35.778×10^{-09}	12.443×10^{-09}
	Multiplier with p-power gating adder	35.778×10^{-09}	12.389×10^{-09}
	Multiplier with reversible logic adder	35.778×10^{-09}	1.461×10^{-09}
Bough wooly multiplier	Multiplier with n-power gating adder	35.778×10^{-09}	8.168×10^{-12}
	Multiplier with p-power gating adder	35.778×10^{-09}	8.1684×10^{-12}
	Multiplier with reversible logic adder	35.778×10^{-09}	8.1684×10^{-12}
Braun multiplier	Multiplier with n-power gating adder	62.902×10^{-09}	32.113×10^{-09}
	Multiplier with p-power gating adder	35.778×10^{-09}	12.177×10^{-09}
	Multiplier with reversible logic adder	35.778×10^{-09}	1.344×10^{-09}

Table 4: Comparison between power consumption of proposed multipliers using 45 nm

Name of the circuit	Name of the circuit	Average current (A)	Average power (W)
Array multiplier	Multiplier with n-power gating adder	9.9237×10^{-09}	3.8411×10^{-09}
	Multiplier with p-power gating adder	9.9237×10^{-09}	3.983×10^{-09}
	Multiplier with reversible logic adder	9.9237×10^{-09}	363.57×10^{-12}
Bough wooly multiplier	Multiplier with n-power gating adder	9.9237×10^{-09}	310.23×10^{-15}
	Multiplier with p-power gating adder	9.9237×10^{-09}	310.23×10^{-15}
	Multiplier with reversible logic adder	9.9237×10^{-09}	310.23×10^{-15}
Braun multiplier	Multiplier with n-power gating adder	9.9237×10^{-09}	5.4887×10^{-09}
	Multiplier with p-power gating adder	9.9237×10^{-09}	4.5634×10^{-09}
	Multiplier with reversible logic adder	9.9237×10^{-09}	424.24×10^{-12}

Table 5: Comparison between power consumption of conventional and proposed mac using 32 nm

Name of the circuit	Power (W)	Average current	Average power
Conventional MAC Unit	125.29×10^{-06}	124.32×10^{-06}	19.02×10^{-06}
Proposed MAC Unit	1.25×10^{-03}	676.23×10^{-06}	4.66×10^{-06}

Table 6: Comparison between power consumption of conventional and proposed mac using 45 nm

Name of the circuit	Power (W)	Average current	Average power
Conventional MAC Unit	143.78×10^{-06}	139.66×10^{-06}	17.39×10^{-06}
Proposed MAC Unit	65.71×10^{-06}	29.51×10^{-06}	11.65×10^{-06}

adder is utilized in the multiplier proposed for the MAC unit of the DWT architecture. The adders and multipliers are designed in 32 nm and 45 nm CMOS technology. For implementation, HSPICE is used.

In the future, circuits will be implemented in FinFET technology. Since the FinFET based technology reduces the second order effects happening in the CMOS devices, the future work will be on the multigate devices.

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